Volume: 09 Issue: 05 Pages: 3563-3570(2018) ISSN: 0975-0290

Design of Low Noise Amplifier using Positive Feedback Gain Enhancement Technique

Dr. P. Kannan
Professor, Head, Department of ECE, PET Engineering College,Vallioor
deepkannan@yahoo.co.in
A. Antony Licy
PG Scholar, Department of ECE, PET Engineering College, Vallioor
antonylicy@gmail.com
Dr. R. Shantha Selva Kumari
Senior Professor and Head, Department of ECE, MEPCO Schlenk Engineering College, Sivakasi
rshantha@mepcoeng.ac.in

ABSTRACT

Low Noise Amplifier (LNA) is a digital amplifier that amplifies a completely low strength signal without drastically degrading its sign to the noise ratio. It's far in any other case known as block down converter. Its miles designed to decrease the additional noise. Here, the low noise amplifier (LNA) is designed the use of a new configuration of high-quality remarks advantage enhancement technique that's suitable for low energy and coffee noise packages. On this proposed technique, additional wonderful comments capacitor is attached to any of the transistor terminal, which will increase voltage benefit due to reducing the entire transconductance. The everyday amplifier circuit is designed the use of energy constrained simultaneous noise and input matching (PCSNIM) method. This technique is used to gain simultaneous enter impedance and minimal noise matching. By means of using this advantage stronger method, the gain of the LNA has been elevated and noise parent is reduced without sacrificing bandwidth, linearity and electricity intake. In this paper we attain 8.620 dB of gain at 4GHz frequency by way of the usage of superb feedback capacitor and interstage matching inductor and also the design of Ultra Wide Band (UWB) LNA provides 14.62dB gain by using inductive source degeneration topology.

Keywords- **Block down Converter, Gain, Positive feedback, Transconductance**

Date of Submission: Feb 10, 2018 Date of Acceptance: March 07, 2018

I. INTRODUCTION

Low Noise Amplifier is an electronic amplifier that amplifies a completely low energy sign without notably degrading its signal to noise ratio. The main requirement of Low Noise Amplifier is low noise determine and high advantage. Parameters like benefit, noise discern, balance and linearity are analyzed to determine the performance of low noise amplifier. Because of the blessings of low price and excessive integration, CMOS generation is widely used in Low Noise Amplifier design. In earlier days 0.35 µm CMOS and 0.18 µm CMOS technologies have been used. Due to the ensuing benefits of decreased chip length, 0.13 µm generation is used these days. It covers the frequency variety of many popular Wi-Fi merchandise together with mobile phones, GPS and Bluetooth.

II. LITERATURE SURVEY

Andrew N.Karnanicolas et al (1996) have supplied layout of RF front stop that includes CMOS Low Noise Amplifier (LNA) and mixer. modern reuse technique is used for growing transconductance of the amplifier. This technique is used to reduce the contemporary consumption of the amplifier and mixer. This measures the electricity benefit and noise discern of LNA at 900MHz [2].

Ming-Dou Ker et al (1997) have provided layout of ESD clamp circuit. This measures the ESD protection performance of submicron of CMOS IC's. This performance relates without delay o pin region of the chip 0.8µm CMOS era which is used to put into effect the layout[5].

Ali Hajimiri et al (1999) have propounded phase noise of differential pass coupled inductance-capacitance(LC).This paper indicates the effects of tail present day and tank strength dissipation on the voltage amplitude. Right here complementary pass coupled pair noise sources are analyzed and their section noise overall performance is diagnosed. Desirable predictions are done for big present day and deliver voltage. on this paper -121dBc/Hz segment noise established for 1.8GHz LC oscillator by using the use of on-chip spiral inductors[1].

Derek K.Shaeffer et al (2005) have presented a paper wherein low noise amplifier approach at 1.5GHz frequency is used for worldwide Positioning system. Implementation of GPS receiver is used a 0.6µm CMOS era it produces a 22dB gain, 3.5dB noise discern and the energy consumption is 30mW from a 1.5v deliver[3].

Yu-Da Shiu et al (2007) have proposed ESD protection circuit and matching network combination of designing a power amplifier (PA). It's been carried out via the use of 0.18 µm CMOS technique. Person I/O ESD clamps are neglected inside the matching network. This generation

Volume: 09 Issue: 05 Pages: 3563-3570(2018) ISSN: 0975-0290

additionally relies upon on Human body model (HBM) ESD robustness on RF performances [11].

Vaithinathan.V et al (2012) have propounded an ultra huge Band(UWB) programs based on two Low Noise Amplifiers(LNA's).One is used without comments topology and different is shunt partial comments topology. On this paper 90nm CMOS generation is used for studying the overall performance parameters consisting of electricity benefit, noise figure and so on. , running at 1V energy supply[10].

J.Sam Hamidon et al (2014) have supplied unmarried degree low noise amplifier(LNA) layout based on the technique of L-matching networks. This technique is used for WIMAX programs. The L-matching community includes lump reactive elements on the enter and output terminals. 18.34dB of strength advantage and 1.34dB of noise parent are accomplished on this layout. Moreover, -16.25dB of input mirrored image and -7.52dB of output go back loss also are received .In this method the amplifier records the bandwidth in the variety of 1.24GHz [9].

III. PROPOSED METHOD

The survey papers mentioned above have a few drawbacks such as Low advantage, balance problem, huge chip place, increased noise determine. The proposed low noise amplifier is designed to triumph over the above disadvantage. The proposed low noise amplifier gives high gain, appropriate reverse isolation and reduced noise determine with decreased chip size. The proposed low noise amplifier is designed and simulated using advanced design machine software program.

3.1 LOW NOISE AMPLIFIER CHARACTERIZATION

The Low Noise Amplifier (LNA) is the first benefit level of a receiver. It should meet several specifications at the same time, which makes its design tough. The alerts coming from the receiver antenna are very small, usually from −100dBm (3.2 V) to -70 dBm (0.1 mV) therefore sign amplification is needed before it's miles fed into the mixer. This procedure sets the requirement of a sure advantage to the LNA. The received sign must have a certain sign to Noise Ratio (SNR) with the intention to permit right detection. Consequently, noise brought via the circuit have to be reduced as a good deal as feasible. A big sign or blocker can occur at the enter of LNA. The circuits ought to be sufficiently linear in order to have an affordable signal reception. Reasonable electricity consumption is another constraint for portable and cell packages. The advantage, balance and noise determine of the LNA are usually measured using the scattering parameters (S-parameters).

3.1.1 SENSITIVITY

RF receiver sensitivity quantifies the ability to reply to a weak sign. It's far described because the minimum detectable signal (MDS) electricity degree with the requirement of the required SNR for an analog receiver and bit-mistakes-rate (BER) for a digital receiver.

3.1.2 NOISE FIGURE

The noise of an amplifier can be defined with a parameter called noise discern (NF). NF is defined as the ratio of the to be had signal to noise electricity ratio on the input to the to be had sign to noise power on the output.

$$\text{NF}=\frac{\boldsymbol{P}_{si}/\boldsymbol{P}_{ni}}{\boldsymbol{P}_{s\text{O}}/\boldsymbol{P}_{n\text{O}}} \quad (1)$$

A minimal noise discern can be obtained through properly selecting the supply reflection coefficient of the amplifier, a method that is defined in following sections. The overall noise figure for a series of n cascaded amplifier is,

$$\text{NF}=NF1+\frac{NF2-1}{G_{A1}}+\frac{NF3-1}{G_{A1}G_{A2}}+\frac{NF4-1}{G_{A1}G_{A2}G_{A3}}+... \quad (2)$$

where G_A is the to be had electricity gain. This suggests that the noise contribution from the first degree is significant for the entire amplifier performance. The goal whilst designing LNAs is then to acquire low NF and excessive advantage at the first amplifier degree. Minimum NF and maximum strength benefit cannot be achieved concurrently and mirrored image coefficient ought to be selected as a compromise among noise and advantage performance.

3.1.3 STABILITY

Stability is critical to don't forget when designing microwave transistor amplifiers. If a transistor is unconditionally strong it's going to now not oscillate with any passive termination. Then again a probably risky transistor may be stabilized via including resistive loadings. One way of expressing necessary conditions for unconditional stability is $K>1$

and $|\Delta|<1$

Where

$$\text{K}=\frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2|S_{12}S_{21}|} \quad (3)$$

and

$$\Delta=S_{11}S_{22}-S_{12}S_{21} \quad (4)$$

Other alternative is to use a μ-issue wherein the condition μ>1 alone is sufficient for a circuit to be unconditionally stable.

$$\mu=\frac{1-|S_{11}|^2}{|S_{22}-S_{11}{}^{*}\Delta|+|S_{21}S_{12}|} \quad (5)$$

Volume: 09 Issue: 05 Pages: 3563-3570(2018) ISSN: 0975-0290

If the transistor is doubtlessly volatile balance circles may be drawn inside the smith chart to decide if there are values of and for which the transistor is conditionally solid.

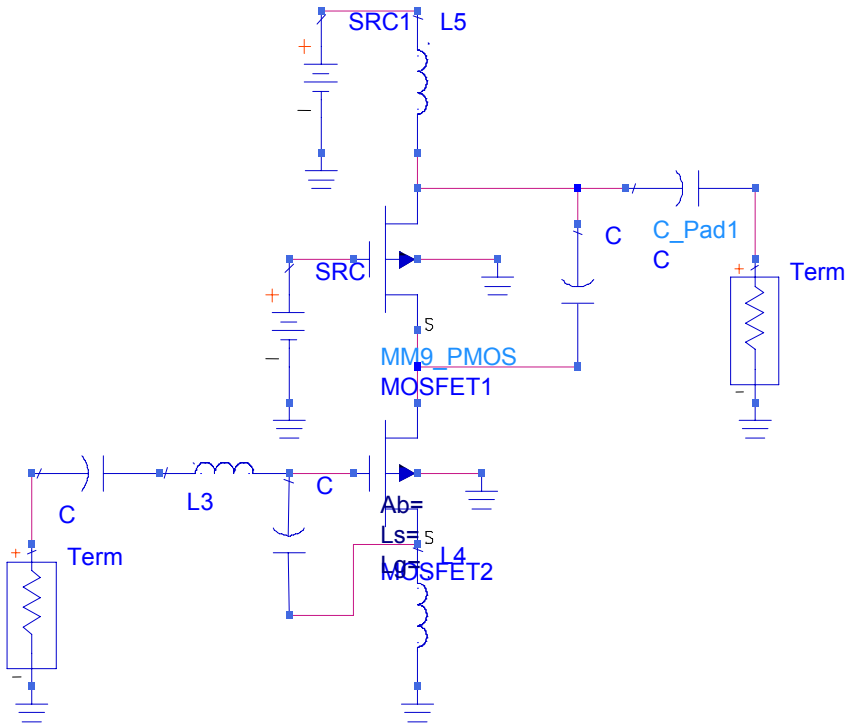
3.1.4 S-PARAMETERS

There are numerous different approaches to signify the behavior of a two port internet paintings. At low frequency, Y, Z, H, T and ABCD parameters are normally used. They use open and short circuit conditions to characterize a linear electrical network. But, these terminations are pretty tough to recognize at high sign frequencies.

In radio frequency variety, scattering parameters (S-Parameters) is normally employed. It makes use of matched load termination and the measurements are based totally on incident and contemplated waves.

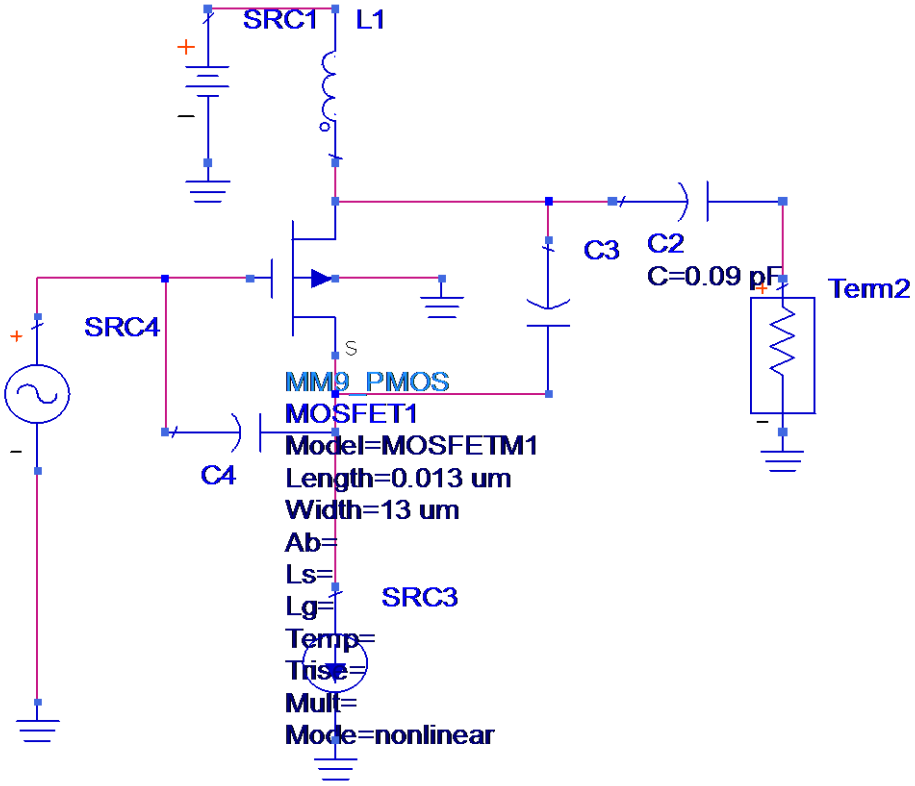
3.2 THE PROPOSED LNA

The LNA with the proposed fine feedback benefit-superior approach is validated in determine three. on this topology, a fine comments capacitance C_f is inserted among the source and drain terminal of the transistor M2. This phenomenon can be understood by using any other factor of view as the form of oscillator. The capacitors C_{gs2}, C_f and transistor M2 represent an oscillator topology with inductive termination at the output.



(a)

Volume: 09 Issue: 05 Pages: 3563-3570(2018) ISSN: 0975-0290



(b)

Fig.1 (a)LNA with the proposed advantage enhancement structure, (b) simplified equal circuit of determine (a).

G_{tot} is the total transconductance on the drain of M2 and is dominated with the aid of the equal parallel conductance of the inductor (G_p).

$$G_p = {}^{1}/_{Q_{L1}^2}\ R_{L1} \tag{6}$$

where in RL1 and QL1 are the series resistance and exceptional element of inductance L1, respectively. further, the LNA gain is proportional to the inductors first-class element and the inductor value as shown beneath:

$$Gain\ \alpha\ R_P\ \alpha\ Q^2\ L_1 R_{L1}\ \alpha\ \omega_0 Q L_1 L_1 \tag{7}$$

Where in RP is the parallel resistance of L1 obtained from the collection to parallel transformation. The above analysis shows that the gain of the circuit may be accelerated through large $G_{m,eff}$ or larger L1.

Assume that $\omega_0 g_{m2}/(C_{gs2} + C_f)$, from the Figure 3 (b), the negative conductance is generated by C_f is,

$$G_N = \omega_0{}^2\, C_{gs2}(C_N + C_{gd2})/g_{m2} \tag{8}$$

So the total transconductance now can be expressed as

$$G\ \hat{}\ \text{tot} = G_P - G_N \tag{9}$$

The gain of the LNA with a feedback capacitance becomes

$$A'_v = g_{m1} Q_{in} \left(\frac{1}{G\hat{}_{tot}}\right) = G_{m,eff} \left(\frac{1}{G\hat{}_{tot}}\right) \tag{10}$$

The A'_v of the cascode LNA with the proposed approach has the same expression as Av (benefit of the LNA without remarks) but with extraordinary G_{tot} is defined by way of the above equation. It's far located that the overall transconductance from the drain of M2 lower with the aid of instances with the increasing remarks, while those from C_f increase. Considering the fact that no energetic device is used, this doesn't boom the energy consumption and additional noise. Consequently, the proposed topology gives plenty higher voltage gain with a help of elevated output impedance. However, the variant of capacitance will slightly change the matching bandwidth. More critical is that massive capacitance can deepen comments degree, for what is going to degenerate the gain and the steadiness of the LNA. Furthermore, the selection of C_f need to don't forget the performance of stability of the LNA as well as the slight benefit.

Volume: 09 Issue: 05 Pages: 3563-3570(2018) ISSN: 0975-0290

IV. RESULTS AND DISCUSSION

The proposed LNA is designed and simulated using PCSNIM 0.18µm CMOS technology in advertisements. S-parameters provide useful performance measures for proposed LNA together with benefit (S21), opposite isolation (S12) and input/output go back loss (S11, S22). Voltage advantage is an essential performance measure of LNA and is calculated the use of the formulation,

$$Gain = 20\log\left(\frac{V_{out}}{V_{in}}\right) \quad (11)$$

In this proposed design, the benefit cost is improved through inter-stage matching inductor L_m at low bias voltage. The voltage gain of the LNA is shown inside the figure 2 which is given beneath:

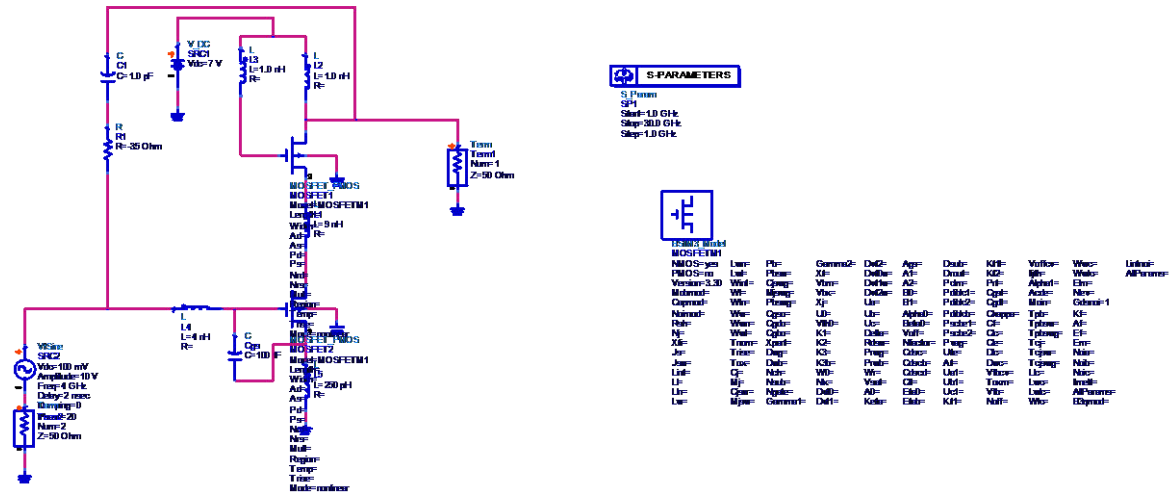


Fig. 2 Proposed LNA

however this utilization is, strictly speaking, wrong based totally at the definition of loss.

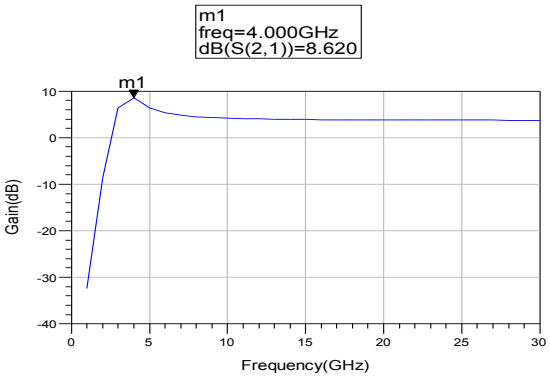


Fig.3 Gain Vs Frequency

Input return loss may be concept of as a measure of the way close the real input impedance of the network is to the nominal machine impedance price. Input return loss is expressed in decibels. Go back losses are now and again used because the poor of the amount described above,

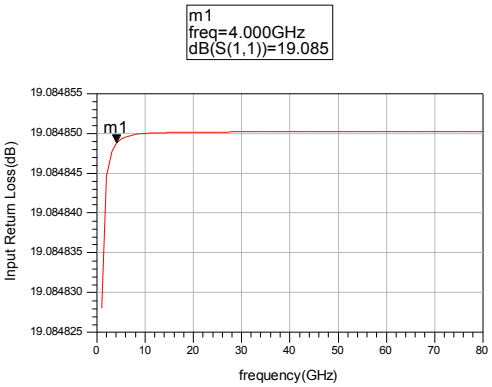


Fig.4 Input Return Loss Vs Frequency

Volume: 09 Issue: 05 Pages: 3563-3570(2018) ISSN: 0975-0290

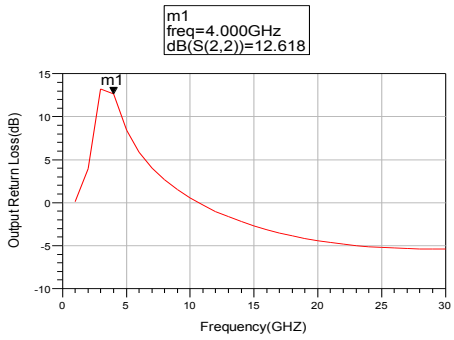


Fig.5 Output Return Loss Vs Frequency

Output go back Loss Vs Frequency reverse isolation is a degree of ways properly a sign applied to the tool output is "isolated" from its input. The size of reverse isolation is much like that of forward gain, except: The stimulus sign is carried out to the amplifier's output port. The response is measured on the amplifier's input port. The equivalent S-parameter is S12. The opposite isolation of the LNA is shown in the figure 6, That is given underneath:

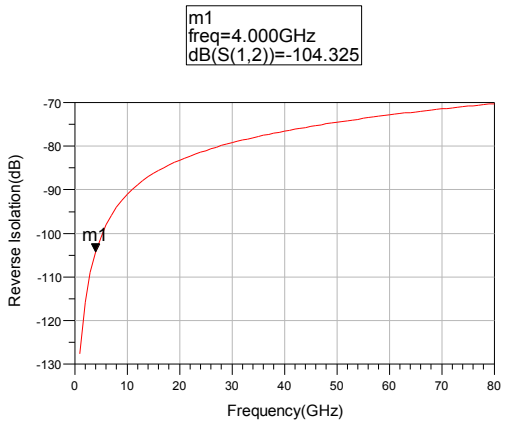


Fig.6 Reverse Isolation Vs Frequency

Noise figure is some other crucial degree of LNA. Normally the noise figure is described as the ratio of sign to noise ratio at the input to the signal to noise ratio on the output and is expressed in dB. The noise determine is calculated the use of transistor small signal parameters. Because of the addition of inductance Lp at the gate of CG degree, the noise figure is decreased. The finished noise discern is shown within the discern 7, that's given beneath:

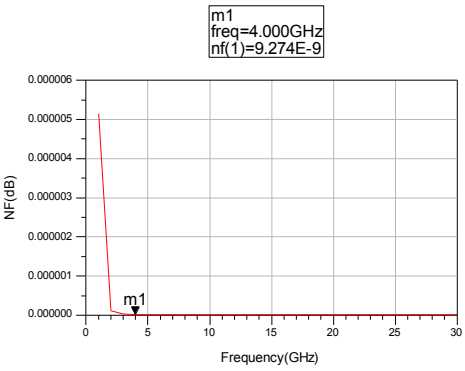


Fig.7 Noise Figure Vs Frequency

Within the proposed LNA the gain cost is 8.620 dB however in tradional LNA the advantage price is 4.733 dB.

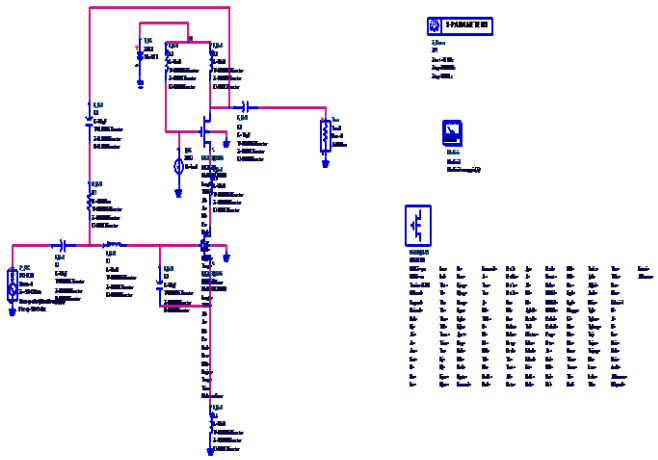


Fig.8 Design of UWB LNA at 5GHz

Volume: 09 Issue: 05 Pages: 3563-3570(2018) ISSN: 0975-0290

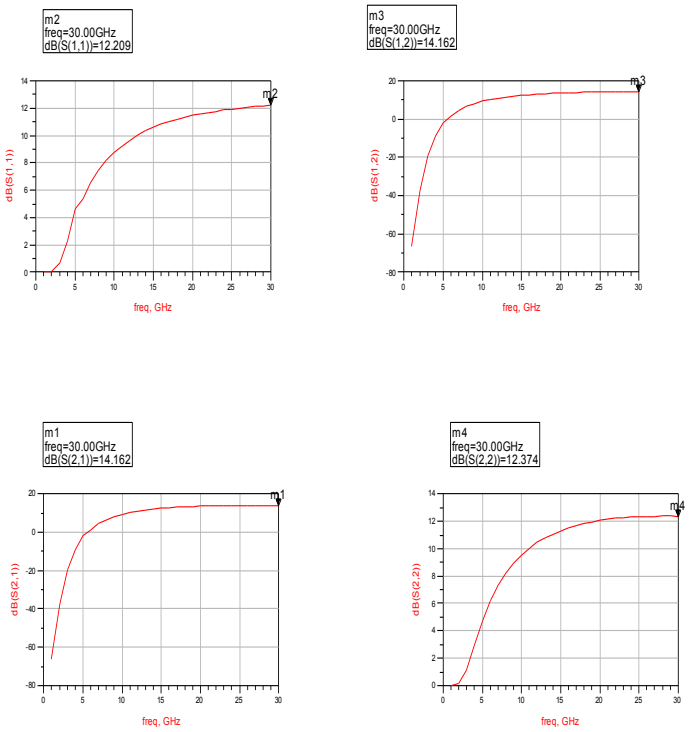


Fig.9 S-Parameters of UWB LNA at 5GHz

The proposed LNA of UWB provide sufficient gain, reduce noise figure with low power consumption.

V. CONCLUSION AND FUTURE ENHANCEMENT

A two stage common supply - commonplace gate low noise amplifier is designed and simulated the use of PCSNIM 0.18µm CMOS era in superior design device. The proposed LNA achieves high benefit, low noise parent and appropriate reverse isolation with low power consumption for Wi-Fi sensor and actor community packages. The advantage of LNA can be substantially improved because of a further wonderful capacitor, which decreases total transconductance of the transistor. The usage of a 0.18µm CMOS procedure, the LNA topology achieves a strength benefit of 8.66 dB at the running frequency of 4GHz. The LNA makes use of a differential topology to boom the linear gain and decide the losses. The duration of the all transistors undertake the minimum channel period to attain a higher cutoff frequency. The cascode topology is selected for this design as it offers better strength gain and better reverse isolation. The proposed Low noise amplifier is useful for low power and wi-fi sensor and actor network packages.

Simulation result has proven that, the advantage of the LNA may be extensively advanced. The proposed low noise amplifier is designed for narrowband application best. The low noise amplifier can be designed for ultra wideband applications additionally the usage of some other technique. The work which has been performed up to the modern-day level indicates that the advantage fee is 14.62 dB. The output of our proposed method bear in mind simplest for improving the advantage. Some of MOSFETs are connected in cascode inorder to improve the gain and also to enhance the noise determine value so as to be taken into consideration in our destiny paintings.

Development of destiny work may encompass enhancing the linearity and bandwidth. A device version for the MOSFET would want to be obtained inorder to simulate the linearity. the size discount of the transistor making the simultaneous noise and enter matching might additionally be considered within the destiny work.

Volume: 09 Issue: 05 Pages: 3563-3570(2018) ISSN: 0975-0290

ACKNOWLEDGEMENT

We thank PET Engineering College for the motivation and encouragement for giving the opportunity to do this research work as successful one.

REFERENCES

[1] Ali Hajimiri and Thomas H.Lee, 'Design Issues in CMOS Differential LC Oscillators', *IEEE Journal of Solid State Circuits,* May 1999, *vol.34,no. 5.*

[2] Andrew N. Karanicolas,' A 2.7 V 900 MHz CMOS LNA and Mixer', *IEEEJ. Solid state circuits, vol. 31, no.12,* Dec.1996, pp. 1939-1944.

[3] Derek K. Shaeffer, and Thomas H. Lee.: 'Corrections to A 1.5-V, 1.5-GHz CMOS Low Noise Amplifier', *IEEE J. Solid-State Circuit,* 2005, 40, (6), pp. 1397–1398.

[4]Md Rahan Chowdhury, Malik Quamrus Samawat, Irtiza Ahmed Salman,' An Ultra-Wide-Band 2.66 - 3.75 GHz LNA in 0.18-µm CMOS Radio Frequency', *International Journal of Engineering Research and General Science Volume 5,* Issue 3, May-June, 2017 ,ISSN 2091-2730

[5] Ming – Dou Ker and Shue-Chang Liu, 'Whole – Chip ESD Protection Design for Submicron CMOS VLSI', *IEEE International Symposium on Circuits and Systems*, June 9-12,1997.

[6]M.Ramana Reddy, Dr. N.S Murthy Sharma, Dr. P. Chandra Sekhar,' A 3.5 GHz Low Noise, High Gain Narrow Band Differential Low Noise Amplifier Design for Wi-MAX Applications', *International Journal of Electronics Engineering Research. ISSN 0975-6450 Volume 9,* Number 4 (2017) pp. 505-516

[7]Nikola Petrović, Radivoje Djurić,' A 94GHz low power UWB LNA for passive radiometer', *INFOTEH-JAHORINA Vol. 16,* March 2017.

[8]Pramod K. B., Kumaraswamy H. V.,' The Linear, Non-linear Measurements, Analysis and Evaluation for the Design of Ultra-Wideband Low Noise Amplifier', *International Journal of Computer Applications (0975 – 8887) Volume 158 – No 6,* January 2017

[9] Sam HamidonJ.,et al., 'Design of Single Stage LNA using L-Matching Network for WIMAX Applications', *ARPN Journal of Engineering and Applied Sciences,vol. 9,*no.10,Oct.2014,ISSN 1819-6608.

[10]Vaithinathan.V, Raja.J and Srinivasan .R, 'A Low Power ,High gain, Low Noise Amplifier with improved noise figure and input matching for Ultra Wide Band Applications', *IJST ,Transactions of Electrical Engineering,vol.36,no,E2,*pp 163-174,2012.

[11]Yu-Da Shiu et al., 'CMOS Power Amplifier with ESD Protection Design Merged in Matching Network', *IEEE Journal of Solid State Circuits,*2007.

[12]Zaid Albataineha, Yazan Hamadeh, Jafar Moheidat, Ahmad Dagamseh, Idrees Al-Kofahi, Mohammed Alsumady,' A High-Gain Low Noise Amplifier for RFID Front-Ends Reader', *Jordan Journal of Electrical Engineering* ISSN (Print): 2409-9600, ISSN (Online): 2409-9619

AUTHOR DETAILS

Dr. P. Kannan (Pauliah Nadar Kannan) received the B.E. degree from Manonmaniam Sundarnar University, Tirunelveli, India, in 2000, the M.E. degree from the Anna University, Chennai, India, in 2007, and the Ph.D degree from the Anna University Chennai, Tamil Nadu, India, in 2015. He has been Professor and Head with the Department of Electronics and Communication Engineering, PET Engineering College Vallioor, Tirunelveli District, Tamil Nadu, India. His current research interests include computer vision, biometrics, and Very Large Scale Integration Architectures

A. Antony Licy (M. Antony Shiril) completed B.E (Electronics and Communication Engineering) in 2016 from Anna University, Chennai. She has published 2 papers in National and International Conference proceedings. Her area of interest include Electronic System Design, Signal Processing, Image Processing and Digital Communication.

Dr. R. Shantha Selva Kumari (Rama Packiam) received the B.E. degree from the Bharathiyar University, Tamil Nadu, India, in 1987, the M.S. degree from the Birla Institute of Technology, Pilani, India, in 1994, and the Ph.D. degree from the Manonmaniam Sundarnar University, Tirunelveli District, Tamil Nadu, India, in 2008. She is currently working as Senior Professor and Head in the Department of Electronics and Communication Engineering at MEPCO Schlenk Engineering College,Sivakasi, TamilNadu, India. His research interests are in bio signal processing and digital communication.