

Improvement of Power Quality by Hybridized Seven Level Inverter

Ashok Kuncham¹ | Md.Shameem²

^{1,2} Department of EEE, Amrita Sai Institute of Science and Technology, Vijayawada, Andhra Pradesh, India.

To Cite this Article

Ashok Kuncham and Md.Shameem, "Improvement of Power Quality by Hybridized Seven Level Inverter", *International Journal for Modern Trends in Science and Technology*, Vol. 04, Issue 02, February 2018, pp.-06-10.

ABSTRACT

Distributed generation (DG) with converter interface to the grid is found in many of the green power resources applications. This paper presents a novel single phase seven level inverter to reduce harmonic content in output voltage and load current. Level shifted multi carrier pulse width modulation (LS-PWM) is used as the switching scheme for the proposed inverter. The validity of proposed inverter is verified through simulation for RL load.

KEYWORDS: Distributed power generation, multilevel inverter, LS-PWM, modulation index

Copyright © 2018 International Journal for Modern Trends in Science and Technology
All rights reserved.

I. INTRODUCTION

A renewable energy application such as photovoltaic (PV) system has been widely used for a few decades since PV energy is free, abundant and distributed throughout the earth. The focus of the Engineers is to make use of abundantly available PV energy and so to design and control an inverter suitable for photo voltaic applications. Power electronic circuits with pulse width modulation (PWM) are mostly used in energy conversion systems to achieve closed loop control. But even updated pulse width modulation (PWM) techniques do not produce perfect response which strongly depends on the semiconductors switching frequency. Also, it is well known that distorted voltages and currents waveforms produce harmonic contamination, additional power losses, and high frequency noise that can affect not only the load power but also the associated controller. The conventional single-phase inverter topologies for driving induction motor include half bridge and full bridge [1]. They are transformer less configuration.

The half-bridge inverter is configured by one capacitor arm and one power electronic arm. The output ac voltage of the half-bridge inverter is two levels. The full- bridge inverter is configured by two power electronic arms. The popular modulation strategies for the full-bridge inverter are bipolar modulation and uni-polar modulation [2]. The output ac voltage of the full-bridge inverter is two levels if the bipolar modulation is used and three levels if the uni-polar modulation is used. Bipolar modulation has less leakage current, but causes more harmonics and more losses.

In order to reduce the losses, uni-polar PWM (Pulse width modulation) is commonly used. All power electronic switches operate in high switching frequency in both half -bridge and full bridge inverters. The switching operation will result in switching loss. The loss of power electronic switch includes the switching loss and the conduction loss. The conduction loss depends on the handling power of power electronic switch. The switching loss is proportional to the switching frequency, and the current of the power electronic switches. The power efficiency can be advanced if the switching

loss of the dc ac inverter is reduced. On the other hand, the power converter technology is continuously developing, and cascaded multilevel inverters have become a very attractive solution for EV applications, due to its modular structure, higher voltage capability, reduced common mode voltages, near sinusoidal outputs, and smaller or even no output filter [8]. In general, cascaded multilevel inverter may be classified in two groups. The first one refers to the amplitude of isolated DC sources devoted to supply each H-bridge cell. If the amplitude of all sources is equal, then the inverter is called symmetrical, otherwise, if at least one of the sources present different amplitude, then it will be called asymmetrical. The second classification label the multilevel inverter whether hybrid or not. If the converter is implemented with different technologies of semiconductor devices (IGBTs, SCRs, GTOs, IGCTs), different nature of DC sources (fuel cells, batteries and super capacitors) and/or if it presents a hybrid modulation strategy, then it is classified as hybrid [9-10].

II. PROPOSED SEVEN LEVEL TOPOLOGY

Proposed seven level inverter is shown in Fig. 1. It consist of two dc bus of magnitudes E & $2E$, six unidirectional switches (S_1, S_2, S_3, S_4, S_b and S_c) and one bidirectional switch (S_a). Each unidirectional switch consists of an IGBT and a fast recovery freewheeling diode. Fig. 2 shows different structure of bidirectional switch [12].

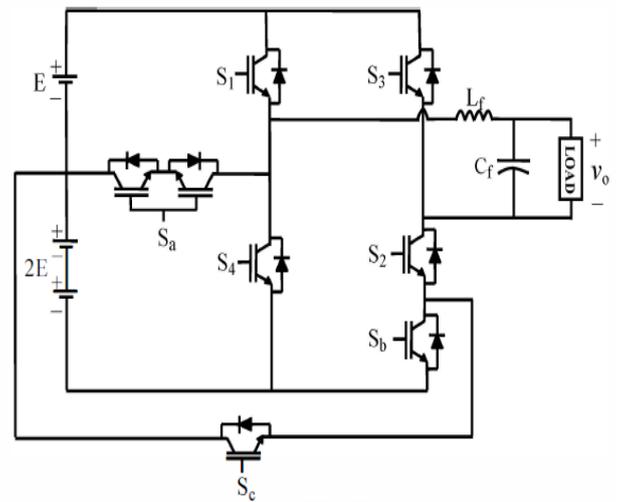


Fig.1: Proposed seven level inverter topology.

Fig. 2(a) requires only one switch and is easy to control, but its voltage drop is high which results in increased power loss. Voltage drop get reduced in Fig. 2(b), but it requires two gate driver circuits. Fig. 2(c) shows common emitter bidirectional switch which require only one gate driver and having reduced voltage drop. Therefore, bidirectional switch in Fig. 2(c) is selected for the proposed inverter. Since the voltage sources are of different magnitude, proposed inverter belongs to hybrid category. By proper switching it is able to generate voltages levels of $0, E, 2E, 3E, -E, -2E$ and $-3E$. Output voltage levels and corresponding status of switches are shown in Table I. The complete operation of proposed inverter can be divided into seven states as shown in Fig. 3. Current path corresponding to seven output voltage levels is also indicated in Fig. 3.

TABLE I
SWITCHING PATTERN FOR PROPOSED INVERTER

S1	S2	S3	S4	Sa	Sb	Sc	Voltage level
1	1	0	0	0	0	1	E
0	1	0	0	1	1	0	$2E$
1	1	0	0	0	1	0	$3E$
1	0	1	0	0	0	0	0
1	0	1	0	1	0	0	$-E$
1	1	0	1	0	0	1	$-2E$
1	0	1	1	0	0	0	$-3E$

Even though proposed topology requires two different dc voltage sources of magnitude E and $2E$, it may be easily realized by suitably arranging dc sources. There is no issue of voltage balancing as no capacitors are used in it. Table 2 shows comparison of proposed topology with other well

known symmetrical 7-level topologies like neutral point clamped (NPC) [1], flying capacitor (FC) [2], cascade H bridge (CHB) [3] and reverse voltage topology [4] in terms of number of components. It is evident from Table II that proposed topology

require less number of components and hence will have reduced switching losses.

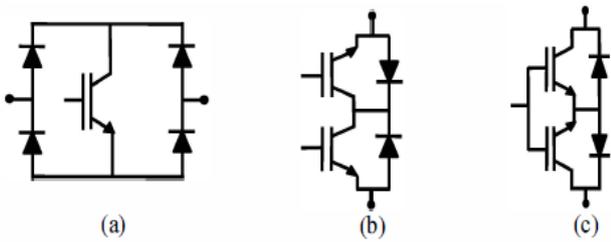


Fig. 2 Bidirectional switch configurations

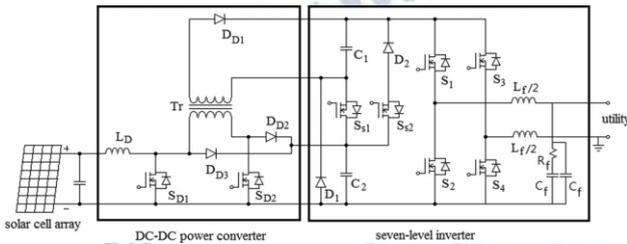


Fig.3: Configuration of the proposed solar power generation system for suppressing the leakage current.

As seen in Fig. 3, the DC-DC power converter incorporates a boost converter and a current-fed forward converter. The boost converter is composed of an inductor L_D , a power electronic switch SD_1 , and a diode, DD_3 . The boost converter charges capacitor C_2 of the seven-level inverter. The current-fed forward converter is composed of an inductor L_D , power electronic switches SD_1 and SD_2 , a transformer, and diodes DD_1 and DD_2 . The current-fed forward converter charges capacitor C_1 of the seven-level inverter. The inductor L_D and the power electronic switch SD_1 of the current-fed forward converter are also used in the boost converter.

III. SIMULINK/MATLAB MODEL OF SEVEN LEVEL INVERTER WITH DC-DC CONVERTER

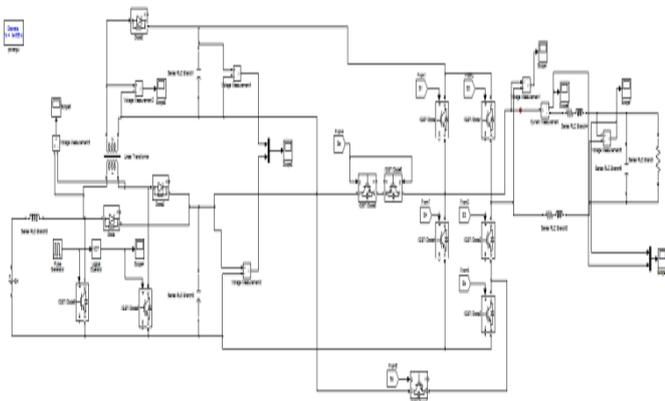


Fig.4: simulink model for proposed seven level inverter with DC-DC converter.

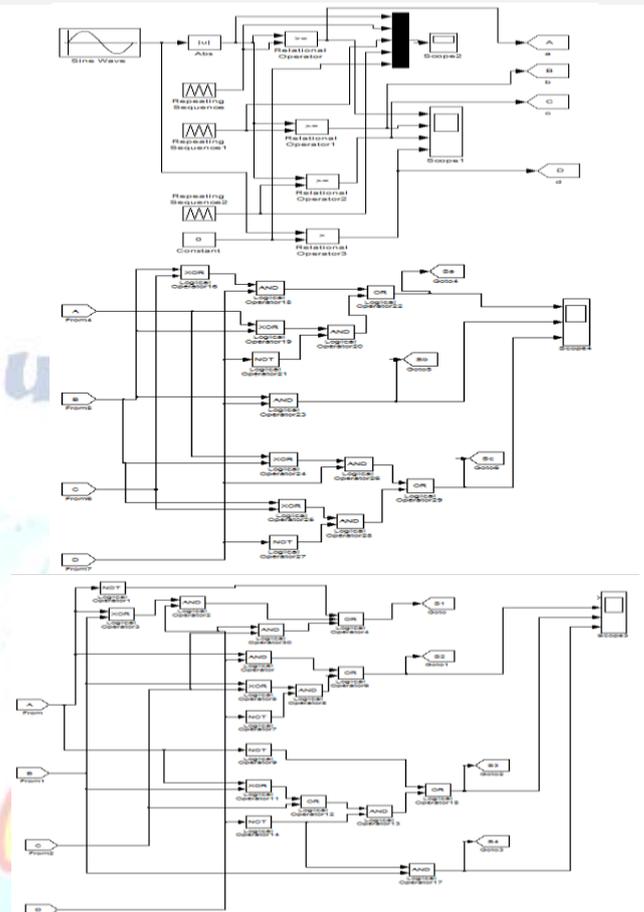


Fig.5: control strategy used to generate the switching pulses.

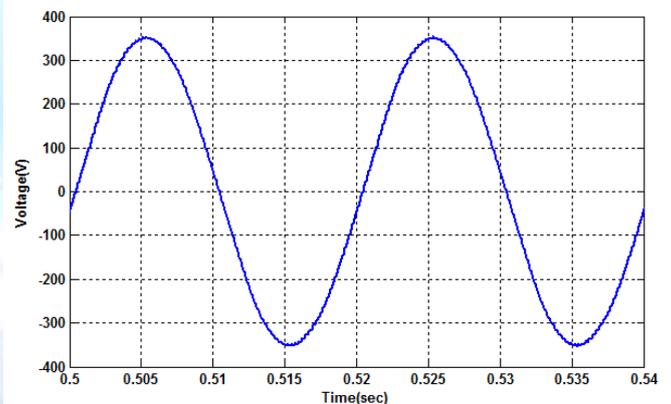


Fig.6: Voltage response in load center.

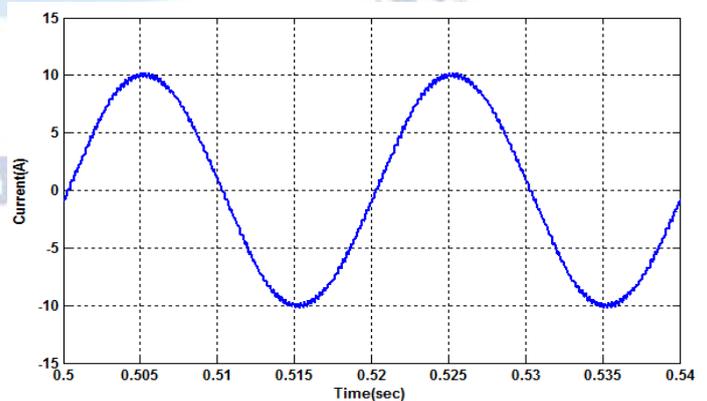


Fig.7: Current response in load center.

IV. CONCLUSION

With the help of proposed inverter topology good power quality is achieved and it can verify by MATLAB software.

Proposed inverter can give yield voltage of good quality with lessened consonant substance. Inverter requires less number of switches which in turn reduces cost and power losses. LS-PWM system is utilized as the tweak conspires for producing pulse signals. It utilizes three carrier signs and one reference flag. Sensible articulations for creating pulse signals from PWM are determined. Execution of proposed inverter system is confirmed through reproduction in MA TLABI SIMULINK.

REFERENCES

- [1]. J. Rodriguez, S. Bernet, P. K. Steimer, and E. Lizama, "A survey on neutral-point-clamped inverters," *IEEE Trans. Ind Electron.*, vol. 57, no. 7, pp. 2219-2230, Jul. 2010.
- [2]. J. Huang and K. A. Corzine, "Extended operation of flying capacitor multilevel inverters," *IEEE Trans. Power Electron.*, vol. 21, no. 1, pp. 140-147, Jan. 2006.
- [3]. E. Villanueva, P. Correa, J. Rodriguez, and M. Pacas, "Control of a single phase cascaded H-bridge multilevel inverter for grid connected photovoltaic systems," *IEEE Trans. Ind Electron.*, vol. 56, no. 11, pp. 4399-4406, Nov. 2009.
- [4]. Ehsan Najafi and Abdul Halim Mohamed Yatim, "Design and Implementation of a New Multilevel Inverter Topology," *IEEE Trans. Ind Electron.*, vol. 59, no. 11, pp. 4148 -4154, Nov. 2012.
- [5]. S. J. Park, F. S. Kang, M. H. Lee, and C. U. Kim, "A new single phase five level PWM inverter employing a deadbeat control scheme," *IEEE Trans. Power Electron.*, vol. 18, no. 18, pp. 831-843, May 2003.
- [6]. Nasrudin A. Rahim, Krismadinata Chaniago, and Jeyraj Selvaraj, "Multistring five-level inverter with novel PWM control scheme for PV application," *IEEE Trans. Ind Electron.*, vol.58, no. 6, pp. 2435 -2443, Jun. 2010.
- [7]. Cas siano Rech and Jose Renes Pinheiro, " Hybrid multilevel converters: Unified analysis and design considerations," *IEEE Trans. Ind Electron.*, 2007, vol.54 no. 2, pp. 1092 -1104, Apr. 2010.
- [8]. Charles 1. Odeh, and Damian B.N. Nnadi "Single-phase 9-level hybridised cascaded multilevel Inverter" ,*JET Power Electron.*, vol. 6, no. 3, pp. 468-477, Jan. 2013.
- [9]. N.A Rahim, Krismadinata, and J.Selvaraj, "Single-phase, seven level grid-connected inverter for photoYoltaic system", *IEEE Trans. IndElectron.*, vol. 58, no. 6, pp. 2435-2443, Jun. 2011.

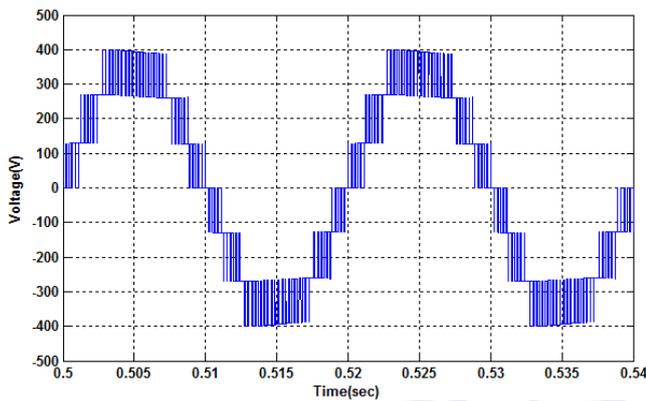


Fig.8: output voltage response of the proposed seven level inverter.

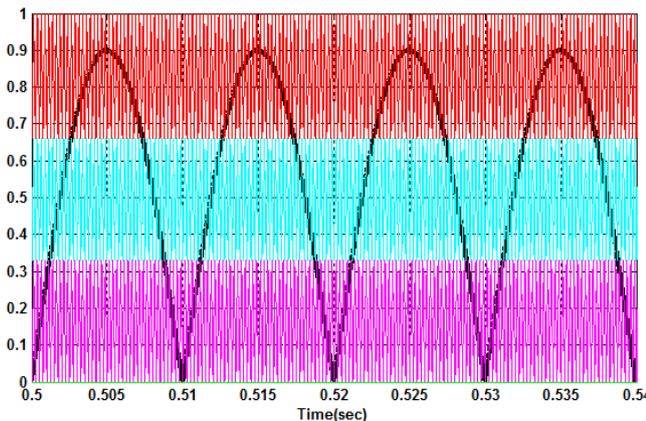


Fig.9 : Response of PWM modulation for $M_a = 0.9$.

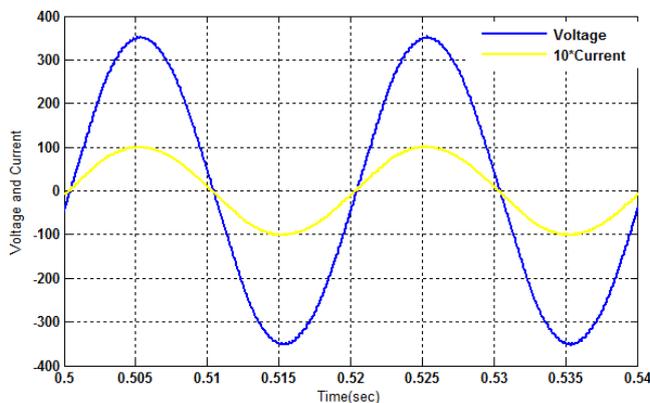


Fig 10: Voltage and current response at the load center.

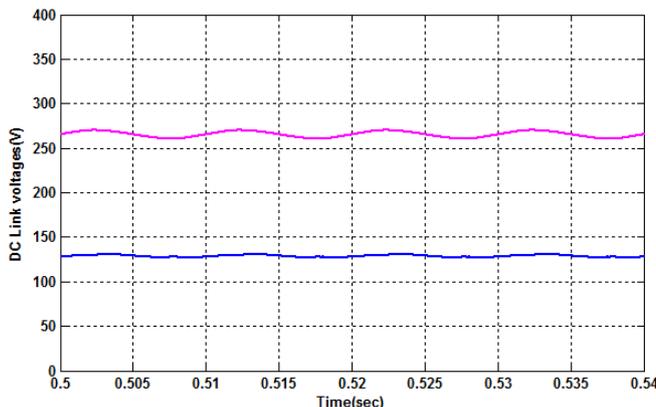


Fig 11: Response of DC link voltage

- [10].K. A. Corzine, M. W. Wielebski, F. Z. Peng, and J. Wang, "Control of cascaded multilevel inverters," *IEEE Trans. Power Electron.*, vol. 19, no. 3, pp. 732-738, May 2004.
- [11].B.P McGrath and D.G Holmes, "Multi carrier PWM strategies for multilevel inverters", *IEEE Trans. Ind Electron.*, vol. 49, no. 4, pp. 858-867, Aug. 2002.
- [12].E. Babaei, "A cascade multilevel converter topology with reduced number of switches," *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 2657-2664, Nov. 2008.
- [13].S. Srikanthan and M. K. Mishra, "DC capacitor voltage equalization in neutral clamped inverters for DSTATCOM application," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2768-2775, Aug. 2010.
- [14].M. Chaves, E. Margato, J. F. Silva, and S. F. Pinto, "New approach in back-to-back m-level diode clamped multilevel converter modeling and direct current bus voltages balancing," *IET power Electron.*, vol. 3, no. 4, pp. 578-589, 2010.
- [15].J. D. Barros, J. F. A. Silva, and E. G. A Jesus, "Fast-predictive optimal control of NPC multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 60, no. 2, pp. 619-627, Feb. 2013.
- [16].A. K. Sadigh, S. H. Hosseini, M. Sabahi, and G. B. Gharehpetian, "Double flying capacitor multi cell converter based on modified phase-shifted pulsewidth modulation," *IEEE Trans. Power Electron.*, vol. 25, no. 6, pp. 1517-1526, Jun. 2010.
- [17].S. Thielemans, A. Ruderman, B. Reznikov, and J. Melkebeek, "Improved natural balancing with modified phase-shifted PWM for single-leg fivelevel flying-capacitor converters," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1658-1667, Apr. 2012.
- [18].S. Choi and M. Saeedifard, "Capacitor voltage balancing of flying capacitor multilevel converters by space vector PWM," *IEEE Trans. Power Delivery*, vol. 27, no. 3, pp. 1154-1161, Jul. 2012.
- [19].L. Maharjan, T. Yamagishi, and H. Akagi, "Active-power control of individual converter cells for a battery energy storage system based on a multilevel cascade pwm converter," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1099-1107, Mar. 2012.

Bibliography



K.ASHOK KUMAR, currently doing his M.Tech at Amrita Sai Institute of Science and Technology. He completed his B.Tech in Sree Venkateswara hindhu college of engineering Machilipatnam. His interested area power electronic converters.



Md.SHAMEEM, received B.Tech degree in E.E.E. Department from SV UNiversity in 2002, Post Graduation in power electronics from Amrita sai institute of science & technology in 2015,. My area of interest is power electronics, electrical machines, and networks. Currently working as a assistant professor in Amrita Sai Institute of Science& Technology.