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FPGA IMPLEMENTATION OF PRIORITY-ARBITER BASED ROUTER DESIGN FOR NOC SYSTEMS

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ABSTRACT

An efficient Priority-Arbiter based Router is designed along with 2X2 and 3X3 mesh topology-based NOC architecture are designed. The Priority –Arbiter based Router design includes Input registers, Priority arbiter, and XY- Routing algorithm. The Priority-Arbiter based Router and NOC 2X2 and 3X3 Router designs are synthesized and implemented using Xilinx ISE Tool and simulated using Modelsim6.5f. The implementation is done by Artix-7 FPGA device, and the physically debugging of the NOC 2X2 Router design is verified using Chipscope pro tool. The performance results are analyzed in terms of the Area (Slices, LUT's), Timing period, and Maximum operating frequency. The comparison of the Priority-Arbiter based Router is made concerning previous similar architecture with improvements.

Keywords—NoC, SoC, Router, FPGA

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1. INTRODUCTION

The increased innovative ideas in the today technology have offered integration of many platforms in one platform. The semiconductor sectors of today's genre are offering efficient and powerful hardware complex structures. Due to the use of these structures the power usage will be optimized. With the increased competition in the complex hardware design, many of the researchers are working towards advancement. Similar way the software usage can be improved with the Computer-aided design (CAD), and it can be developed. A CAD tool has simulation, modeling, implementation and synthesis tools.

The system on chip (SoC) has different processing elements (PE) like intellectual properties (IP), processors, etc., input and output modules for communication and memory blocks. The present technology is very much interested in the on-chip elements.

The SoCs composed of many IP blocks, physical links, and routers. The IP block is used to represent Digital signal processing, MPEG decoders, memory modules, etc. The Links and routers of the SoC are used to build the communication for IP blocks or NoC organization. The routers of the NoC will be connected to the IP blocks using input and output ports. The ports required to build the connection is dependent on network topology.

The every NoC designs exhibit some features of performance factors like throughput, latency, power usage, area, and hardware complexity. The above factors depend on each other, which cannot be used individually. The performance factors can be split as cost and performance parameters. The performance parameters of the NoC are considered as latency and throughput. Generally, the latency considered as the time took to forward the packets to the destination from the source, While the throughput is considered as the part of a packet which is forwarded to the destination in particular time from the source. In any desired applications of the NoC, we need low latency with high throughput. The low latency with the high throughput can be obtained by proper utilization of the channel, implementation of the proper routing algorithm, providing the livelock, deadlock & stardom freedom and by proper switching technique implementation. In this sense there exist cost parameters like hardware complexity, power usage, and area usage. The NoC design for the battery depending applications like mobile devices suffer from power usability. The area is the primary factor in buffer size enhancement from the single router. The buffer size will affect the router area and power usage. These buffers size depends on the type of switching technology adaption and implemented routing algorithm.

The section 2 discuss about the existing works of Router and NoC and Problems finding. The section 3 explains about the proposed Router with descriptions. The results and analysis of the work is elaborated in section 4. Finally concludes the overall system with improvements with future work in section 5.

2. RELATED WORKS

The review of the existing work on RISC Processor architectures and ALU Units are described in below session.

The study of Bhanwala et al. [1] has focused on the design of reconfigurable Network on chip (NOC) application, based on Field propagation array (FPGA). The design of this complete application is done by the using of Verilog hardware description language. The presented design application is worked in four channel east, west, north, and south and also work for a crossbar switch, the presented all channels are work of first in first out multiplexers and buffers. The work of Kapre et al. [2] have concentrated on the making of low cost but an active and high-performance network-on-chip system based on Field propagation array. The quality of FPGA is buffer less, smaller magnitude and run faster-operating frequency that's why it is used with Network-on-chip system. The study of Daf et al. [3] has discussed the evaluation and performance of Loopback Virtual channel router, in which also focused on the working process of a router and discussed the router was helping component during working. The work of Kashwan et al. [4] has concentrated on performance analysis of a new optimized Network-on-chip router, in which using of multiprocessor network on a chip is a proper solution for increasing a higher performance designed with VLSI. The work of Nasir et al. [5] has concentrated on the problem of communication between sources to destination, in which different types of issues come like area, delay, power consumption. For solving this problem presented an Elastic buffering (EB) technique in virtual channelling in an in NoC. In which pipeline flip-flop system is us as a storage location to store data.

The work of Aslam et al. [7] has concentrated on the development of a routing protocol technique for efficient Network on-chip transmission, in here introduce a Junction-based routing protocol about this protocol it is a suitable technique for log Network on chip platforms. The study of Kumar et al. [8] have focused on the design of area-efficient router framework based on FPGA for Network on chip, Once the completing of the design of channels, the crossbar is also designed and after the completing the process of design of crossbar and all four channels both designed are integrated with the making of the framework of a router. The work of Lu et al. [9] have concentrated on the problem of delay in packet transmission and cost in routing, for solving this issue presented a Low-Latency NoC Router framework. The study of Monemi et al. [10] has focused on the problem of a design of less time taking network on the chip with a low area overhead technique. For solving this problem presented a two-clock-cycle latency network on chip micro-framework.

The work of Boutalbi et al. [11] has presented a trustable routing technique for the detection of the online issue in dynamic Network on a chip. The presented technique can fully detection and localization of inner and outer data packet during transmission and detects the error between permanent and temporary error. The study of Wang et al. [12] have focused on the condition of congestion and hot spot in traditional 3D Network on a chip, and this network is not an element of multicast. For solving this hot spot problem in 3D network on chip presented a Multicast Rotational Routing Arithmetic scheme (ARRAs). The work of Salah et al. [13] has concentrated on the design of a scalable routing protocol for packet-switched in the network on chip in the environment of System-on-chip. For the best packet delivery and solving the interconnection issue presented a circuit-switched NoCs to a positive performance and presented quality of service for a system on chip. Abdelrasoul et al. [14] have introduced a re-evaluate framework named Round Robin Arbiter (RRA) based on FPGA to cover this gap. Abdelrasoul et al. [14] have introduced a re-evaluate framework named Round Robin Arbiter (RRA) based on FPGA to cover this gap. The work of Liu et al. [16] have discussed custom-silicon network-on-chip into an FPGA; it's helpful on the communication bandwidth. For the efficient communication presented a mixing Hard Network-on chip technique to focus on the packet switched routing protocol and supported pre-schedule and packet switched communication. The study of Siddhartha et al. [17] have presented a Hoplite-Q, Field propagation Gate Array-based Network on chip routing technique, the presented technique is priority-aware friendly with FPGA its capable to exploiting application priority during routing communication under a workload.

Problem statement: Most of the Existing NOC Router designs are software based and not compactable to the real-time environments. In that, very few are hardware-based approaches and lacks hardware complexities and performance metrics in real time. Most of the NOC Router designs are ASIC Based approaches and limited to perform only a few parameters. Very few NOC Router verification is done on real-time environments and lacks optimizations. To verify the hardware designs with real-time data, it is difficult without using the simulation testbench. The Unit under Test (UUT) is the design module is incorporated in the testbench to verify the designs. But it lacks with controllability in real time.

Proposed Solution: The proposed Priority-arbiter based NOC Router overcomes comes to the problems and improves the NOC performance. The NOC Router Verification is done quickly by using intellectual property (IP) cores. In that, virtual input-output core (VIO) is used which improves the controllability of the NOC in real-time verification.

3. PROPOSED ROUTER

The single router Design which includes Input Registers, Arbiter design, Packet formation, and Routing Algorithm is shown in figure 1. The input register is having five port 16-bit inputs like Packet input (local), east, west, south, and north inputs, these inputs are stored in register

temporarily. Once grants are ready in arbiter and temporary port data signals are stored in the Priority Encoder.

The priority-based arbiter receives the requests from the five port inputs, based on the request, the arbiter checks the all 5 possible states, which state is free to allocate the data based on priority.

The FSM state machine is designed to check the grants based on the requests. Arbiter generates 5- grants which are acts as a 5-bit select line to the priority encoder. Based on the 5-bit select line, the priority encoder will work.

- If the select line is 00001, then packet input is selected.
- If the select line is 00010, then east input is selected.
- If the select line is 00100, then west input is selected.
- If the select line is 01000, then north input is selected.
- If the select line is 10000, then south input is selected.

Based on the priority encoder output, the frame the packet. Then apply the XY routing algorithm to generate the five port output signals to reach the destination.

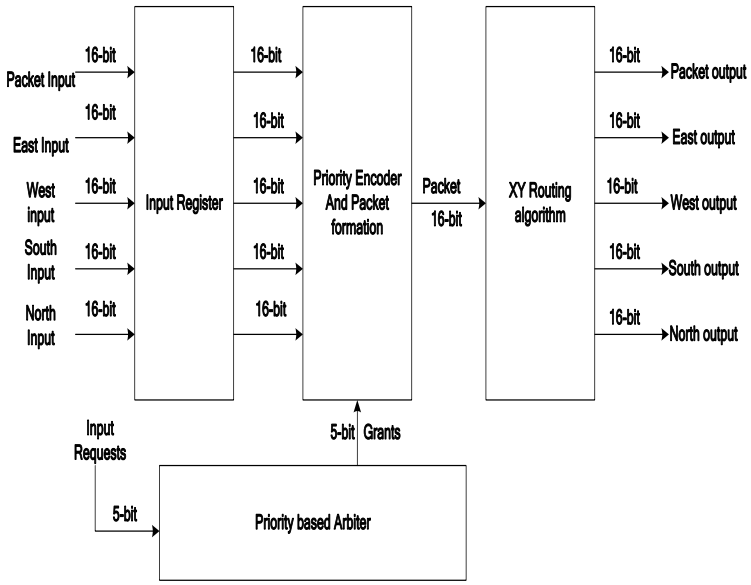

Figure 1 Single-Router Architecture.

The arbiter is used to select the request based on the priority and generates the grants. In figure 2, the arbiter FSM is represented, and it is having three requests (req0, req1, and req2) and three grants (gnt0, gnt1, and gnt2). In FSM, 4 states are there, and it acts as a present and next state. The FSM works based on the binary encoding scheme for states. In design, States are initialized to IDLE = 00, GRANT-0= 01, GRANT-1= 10, and GRANT-2= 11. The arbiter FSM design, first finds the next state and then present state followed by output state.

The next state logic is same as combination logic. In four states, based on the three input requests (req0, req1, and req2), it generates the next state. If the state is IDLE, if the req0=1, then next state is GRANT-0 else, if the req1=1, then next state is GRANT-1 else, if the req2=1, then next state is GRANT-2.

If the state is GRANT-0 is the input state, if the req0=1 then immediately, the next state is GRANT1. Otherwise, if the requests come from the req1 or req2, it will result in the priority

and stores those request temporarily. Once the next state releases the present requests, and it gives priority to the stored temporary requests.

Similarly, If the state is GRANT-1 is the input state, if the req1=1 then immediately, the next state is GRANT2. Otherwise, if the requests come from the req0 or req2, it will result in the priority and stores those request temporarily. Once the next state releases the present requests, and it gives priority to the stored temporary requests.

Similarly, If the state is GRANT-2 is the input state, if the req2=1 then immediately, the next state is IDLE or GRANT0. Otherwise, if the requests come from the req0 or req1, it will result in the priority and stores those request temporarily. Once the next state releases the present requests, and it gives priority to the stored temporary requests.

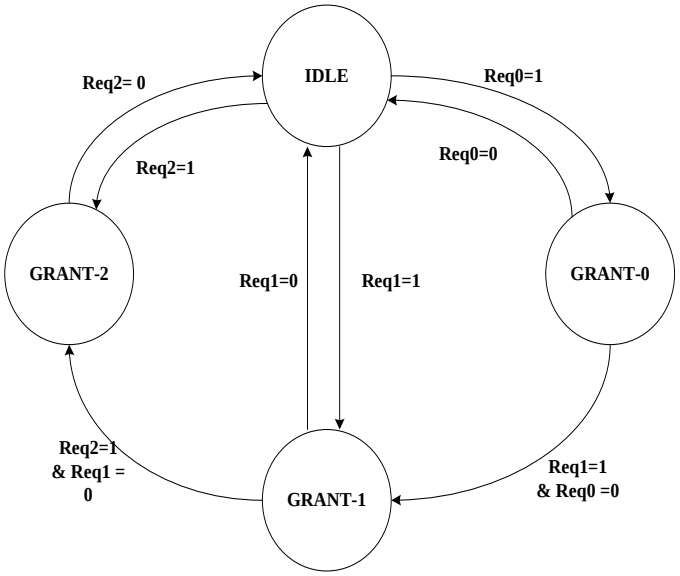

Figure 2 Arbiter FSM Design

In the present state, IDLE is the default state. Based on the next state logic, the present state is generated on every successive clock cycle. In output state, based on the present state inputs, the 4 states generate the grants.

The packet formation is performed based on the priority encoded output data signals. It is having mainly 8-bit packet data (priority encoded data), 3-bit is reversed for future purpose, 2-bit Destination-X address, and 2-bit destination-Y address and 1-bit request.

The XY Routing algorithm is represented Based on the Current and destination address, the framed packet will move X-direction or Y-direction as per algorithm.

- If the destination X (desX) is equal to Current X address and destination Y (desY) is equal to Current Y address, then the local output will be generated.
- In that, if the destination Y (desY) is higher than the Current Y address, then the south output will be generated. Otherwise, if the destination Y (desY) is less than the Current Y address, then north output will be generated.
- Parallelly, if the destination X (desX) is greater than the Current X address, then the east output will be generated. Otherwise, if the destination X (desX) is less than the Current Y address, then the west output will be generated.

The NOC 2X2 router mainly consists of the four individual routers like R1, R2, R3, and R4. Each router has 4-bit XY current address, for Router R1- 00_00, Router R2- 00_01, Router R3- 01_00, and Router R4- 01_01.Based on the XY routing algorithm and destination address the routing operation is performed in the NOC 2X2. For NOC 2X2 Router, for communicating

from one router to another router, linking wires are used. The router R1 receives the data through west input (WI) of R3 and North input (NI) from R2 and generates east output (EO) and south output (SO). Similarly, it is applicable for R2, R3, and R4. For NOC 3X3 Router, it has nine routers R1-R9 which is similar to the NOC 2x2 router. The current -XY address will be changed, and it consists of nine input and nine output ports.

4. RESULTS AND ANALYSIS

The proposed Router results are described detail in the below section. The Complete Router with NoC is designed using Verilog HDL over Xilinx ISE Platform and simulated on Modelsim simulator and Hardware prototyped on low cost Artix-7 FPGA.

The Single router Simulation Results are a representation shown in figure 3. Once clock (clk) is activated with low reset, set the router inputs Local (packet_in), east (pine), west (pinw), south (pins), and north (pinn). After performing the Routing operations based on current and a destination address using XY algorithm, the 8-bit output of data_out (local output and 16-bits east (poe), west (pow), south (pos), and north (pon) outputs are generated.

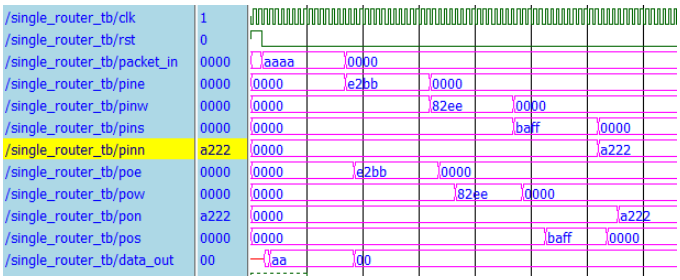

Figure 3 Single router Simulation Results

The proposed Single router is compared with similar previous router [18] concerning resource utilization on same selected Spartan 3E -500 Device FPGA. The improvements in slice Registers around 25 %, slice-FF's around 18%, 4-input LUT's is 11%, and Global Clock is around 17%.

Table 1 Comparison of Single router with previous [18]

Logic Utilization	Available	Proposed Router	Utilization	Router [18]	Utilization
Slices	4656	862	18%	2024	43%
Slice Flip Flops	9312	642	6%	2133	22%
4 input LUTs	9312	1264	13%	2231	24%
bonded IOBs	232	98	42%	74	32%
GCLKs	24	1	4%	5	21%

Overall the Single router is efficient and consumes less resource utilization than previous architecture**.**

5. CONCLUSION

The cost-effective and straightforward Single router along with 2x2 NOC and 3X3 NOC Routers are designed using Verilog-HDL and implemented on Artix-7 FPGA Platform. The Single router mainly contains Input registers, Arbiter, and XY-Routing algorithm. The Hardware architecture of 2x2 NOC using ICON IP Core and VIO IP cores are designed. The simulation results of the NOC Routers is seen using Modelsim 6.5f. The NOC Routers are implemented on Artix-7 FPGA with physically debugging using Chipscope pro tool. The NOC

Routers are synthesized and implemented using Xilinx ISE Tool. The Single Router is compared with previous similar architecture on the same FPGA devices with an Improvement in area overhead of slice Registers around 25 %, slice-FF's 18%, 4-input LUT's is 11% than the previous single router.

In Future, these NoC routers are communicated with network interfaces and processing elements for Systems on chip designs to reduce the chip complexity.

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