POWER-DELAY EFFICIENT ASYNCHRONOUS DESIGN APPROACH USING GALEOR

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ABSTRACT

Leakage power dissipation is a chief alarm in nanometer & deep submicron technologies. In CMOS circuits, leakage current has become major supplier to the whole power dissipation attributable to the unremitting trend of technology scaling. The main objective of this paper is to reduce leakage power dissipation with diverse leakage diminution techniques. We propound a novel seepage decline methodology named "Multi Threshold Null Convention Galeor" which can attain superior leakage power deduction analogize to the other techniques agitate in this paper. In order to extant the rendition of proffer approach, a full adder is schemed and there by demonstrate the power, delay, slew rate and energy. All 27 threshold standard cells are designed and simulated for low power performance; delay evaluation and is presented in this paper.

Key words: Low power loss, Delay, Energy, MTNCL, GALEOR

1. INTRODUCTION

Leakage power dissipation is caviling in semiconductor devices while it leaks the power even through circuits are in dormant state [1]. In VLSI design with the hasty liftoff battery handled applications, power consumption has turned to one of the substantive concern [2]. In order to chalk up lofty performance in CMOS technology threshold voltage has been gauge down. It causes short channel effects which uptick sub threshold leakage current exponentially [3]. This sub threshold leakage current addendums the leakage power. Scheming and developing eminently systematic analog circuits are befitting a strenuous task ahead through the power

reduction [4]. To eschew the liabilities in Multi Threshold Null Convention Logic (MTNCL) and Gated Leakage transistor (GALEOR) techniques, we are cartel these two techniques. This substitutive technique is tattered to diminish power dissipation [5].

For a CMOS circuit, the total power loss is the amalgamation of static and dynamic components. Power dissipation is integrally the rate at which energy is drawn from the power supply, which is commensurable to the average power dissipation [5]. Dynamic power dissipation is caused by gratuitous switching exertion in transistors. The cradles of static power dissipation are p-n junction diode leakage current, band-to-band tunneling current, sub threshold leakage current, hot carrier injection, tunneling through gate oxide, gate induced drain leakage and punch through [6]. Brief of these leakage currents are shown in Fig.1. In Fig1, junction leakage (I1) is garner by reverse bias leakage current spurt between the source/drain and substrate regions. When the transistor is biased in cutoff, it causes sub threshold leakage current (I2).
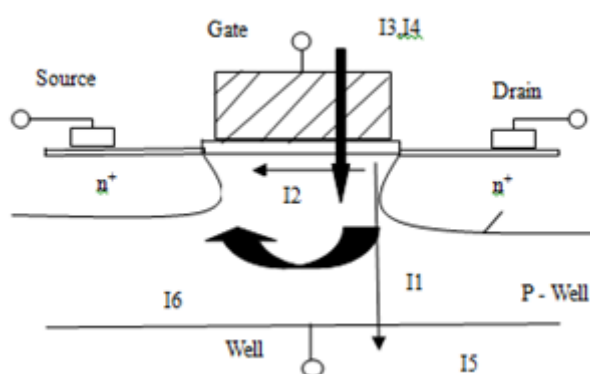

Figure 1 Schematic of Leakage current mechanism of deep - sub micron transistor

When high electric fields are applied across the gate oxide region then the gate oxide leakage (I3) is transpired. Hot carrier injection (I4) is due to the clouded of threshold voltage by electrons/holes ambushed in the oxide layer. Gate induced drain leakage (I5) results consequent of the stirring of minority charge carriers between channel and substrate regions. When channel evanesces, the current pour between sources and drain regions, it causes punch through leakage (I6). Static power dissipation is mostly betiding due to the sub threshold leakage.

The mechanism tangled in dynamic dissipation is short circuit power, switching power and glitching power dissipation. Techniques like NCL [2], MTNCL [3], LECTOR [4], and GALEOR [5] are used for leakage power dissipation. Each technique has its own sustenance's and liabilities. Some methods use low-V_T transistors and high-V_T transistors. Low-V_T transistors are commonly used to design the logic gates where switching speed is necessitous, whereas high-V_T transistors are used to efficaciously anchorite the logic gates in stand-by and to avert leakage dissipation. However, we propose a new leakage power reduction technique for implementing of CMOS circuits combining MTNCL and GALEOR techniques as there are drawbacks in MTNCL and GALEOR techniques individually. To understand and for the benefit of readers, we have presented different leakage reduction techniques in Section 2. Section 3 describes proposed mechanism. Section 4 depicts the results, analysis and comparison with the available techniques. Finally section 5 concludes this paper.

Our proposed Multi threshold null convention Galeor technique demotes power dissipation and meliorates the rendition of the circuit in CMOS circuits and gates. Comparing with MTNCL it is the gaiety technique to bust total power dissipation.

2. PREVIOUS TECHNIQUES

Due to the incessant scaling down of CMOS technology, leakage is becoming cognate to dynamic switching power[6] degrade leakage power dissipation, legion techniques NCL, MTNCL, LECTOR, GALEOR are suggested.

2.1. Null Convention Logic (NCL)

Null convention logic is one of the widely exemplars of asynchronous circuits as shown in Fig.2. NCL is four phase, dual rail logic family based on threshold logic. It can be accustomed to build delay-insensitive systems and CMOS static & semi-static implementations. NCL gates are
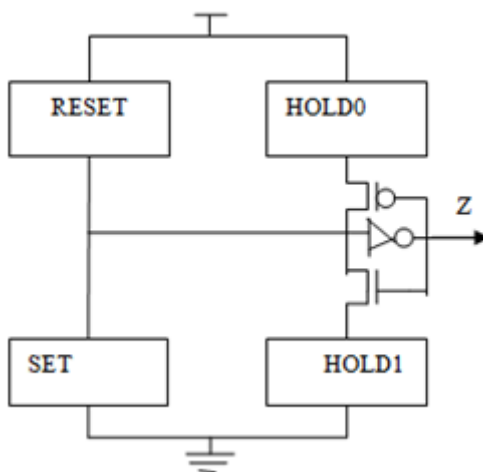

Figure 2 Static Implementation of NCL Logic Gates

schemed using hysteresis state holding functionality. In this static implementation, all the inputs must be reasserted before the output is reasserted and NMOS transistors are placed rather than weak feedback inverter [7]. Here hold0 & hold1 blocks are prescribed to conserving the output values unbothered, and the set and reset transistors are complimented in NCL gates. The two additional blocks are given as hold0=Z set, hold1=Z reset. Some boons of this technique are demoted propagation delay and power consumption. This methodology also suffers in producing faithful voltage levels.

2.2. Multi Threshold Null Convention Logic (MTNCL)

Fig.3 shows Multi threshold null convention logic cartels NCL [7] with MTCMOS [8], to yield less power dissipation. MTNCL technique is also named as Sleep convention logic. This technique does not require any additional hardware because here we use completion detection handshaking signals as the sleep signals. In this technique, due to the mien of sleep signal, fundamental blocks are reduced to two. Therefore, here we use HOLD-0 and SET blocks. Minimize the voltage potential across the HOLD-0 and SET blocks, to reduce leakage. During active mode, sleep signal is logic 0, such that sleep transistors are turned on, bypass transistors are turned off and output transistor is also turned off, such that the circuit functions as normal.
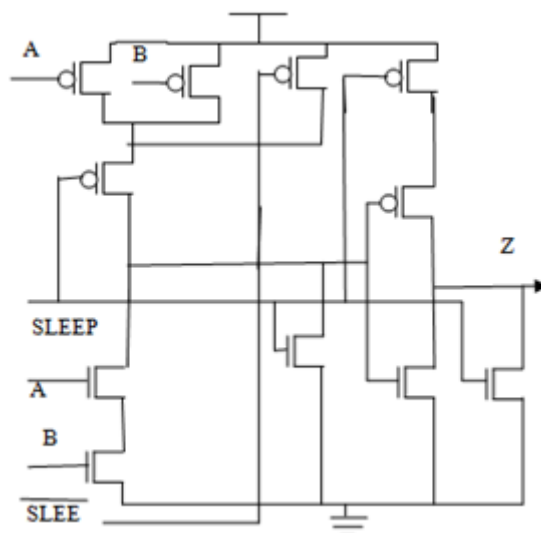
Figure 3 Block Diagram of MTNCL

During sleep mode, sleep is logic 1, such that low threshold voltage transistor is turned on and high threshold voltage gating transistors are turned off to reduce leakage. The implementation of TH22 MTNCL is shown in Fig 4. The Boolean Expression of the TH22 gate is TH22 = AB whose inputs n=2, threshold of the gate m=2. All the threshold gates will become logic 0 when hold1 circuit put into sleep mode, so no longer hysteresis required. In which, hold 0 block represents pull up network and set block represents pull down network. MTNCL approach is the superior technique among all the asynchronous design methodologies [9]. Better performance of MTNCL is degraded due to its glitch phenomenon at its internal nodes. The leakage current between VDD and Vss rails leads to the abnormalities at output levels. These spurious pulses will be suppressed by minimizing leakage currents. LECTOR approach is best apt for reducing leakage currents and thereby to improve the performance of MTNCL.
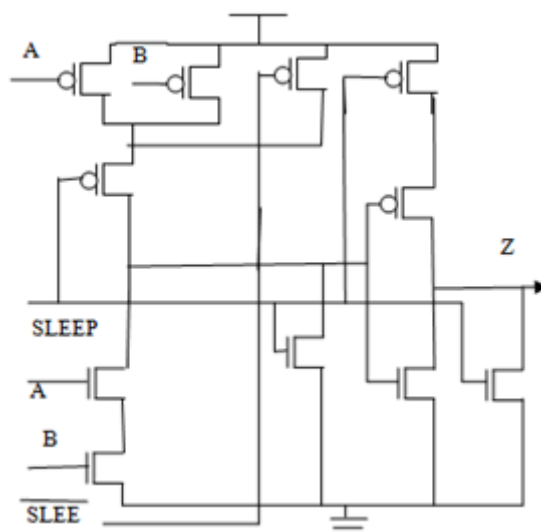

Figure 4 TH22 Gate Implementation using MTNCL

2.3. LECTOR

The assembling of transistors from VDD to GND reduces the leakage power. In this technique, two leakage transistors are stationed between pull-ups and pull down networks. If additionally

one transistor is off in a path from VDD to GND the leakage is inferior. Those LCTs are self-controlled transistors, they do not necessitate any further circuit. LCTs are positioned in between two nodes N1 and N2. These two LCTs addendums the resistance. The gate terminal of LCT1 is connected with the source terminal of LCT2[10]. Similarly, gate terminal of LCT2 is connected with the source terminal of LCT1. Among those two LCTs, one transistor is in cutoff region, this is shown in Fig. 5.

An AND gate with the addition of two leakage control transistors which is known LECTOR AND is shown in Fig 6. In this circuit, LECTOR technique is applied between the pull up and pull down networks. The gates of LCT1 and LCT2 are controlled by the potential at source terminal of LCT2 and LCT1 respectively. Another popular approach for the reduction of leakage current is GALEOR approach.
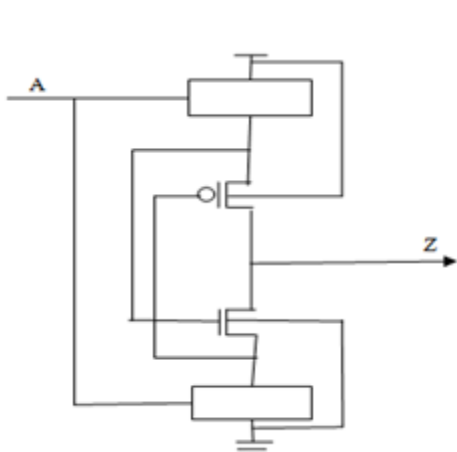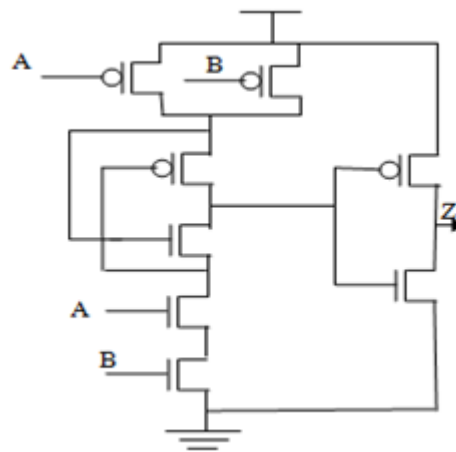

Figure 5 LECTOR CMOS Gate   **Figure 6** AND Gate using LECTOR Technique

2.4. GALEOR

The method shown in Fig.7, insinuate two leakage control high VT transistors between pull-ups and pull down networks. In this technique, a leakage control high VT PMOS transistor is positioned between output and pull down network. Cognately, a leakage control high VT NMOS transistor is placed between output and pull-up network [11]. By acquaint high threshold voltage transistors this method logs paramount reduction in leakage power.
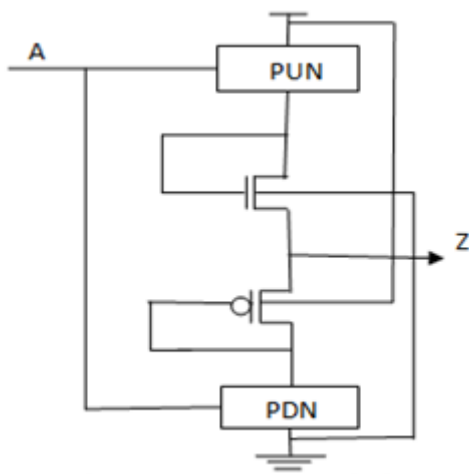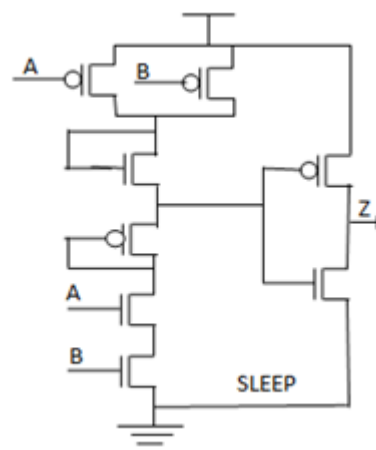

Figure 7 GALEOR Technique   **Figure 8** AND Gate using GALEOR Technique

It reduces the leakage current pouring through the circuit and output voltage swing due to the threshold voltage loss. The main liability in this technique is large static leakage power dissipation in idle mode. 2 input AND gate using GALEOR technique is shown in the Fig 8. In this figure, GALEOR technique is practicable between pull up and pull down networks in which, a high Vt NMOS transistor is placed between output and pull up network and a leakage control high Vt PMOS transistor is placed between output and pull down network.

3. PROPOSED METHODOLOGY

In this district, we acquaint a new leakage power reduction technique for implementing of CMOS circuits. Fig 9 shows the Multi Threshold Asynchronous Galeor technique which syndicates the MTNCL & Galeor techniques. As there are drawbacks in MTNCL and GALEOR techniques, we choose this proposed technique. In this new technique, we have to place the GALEOR technique at the output of the MTNCL.

By presenting high threshold voltage transistors, the maximum reduction in leakage current is achieved. Hence it reduces the leakage current streaming through the circuit. In this method the Galeor provides two leakage control transistors (PMOS & NMOS) within the circuit in which, the gate terminal of each leakage control transistor is prescribed by the source terminal of the other Leakage Control Transistor (LCT).

The LCTs do not require any control logic because they are self controlled.
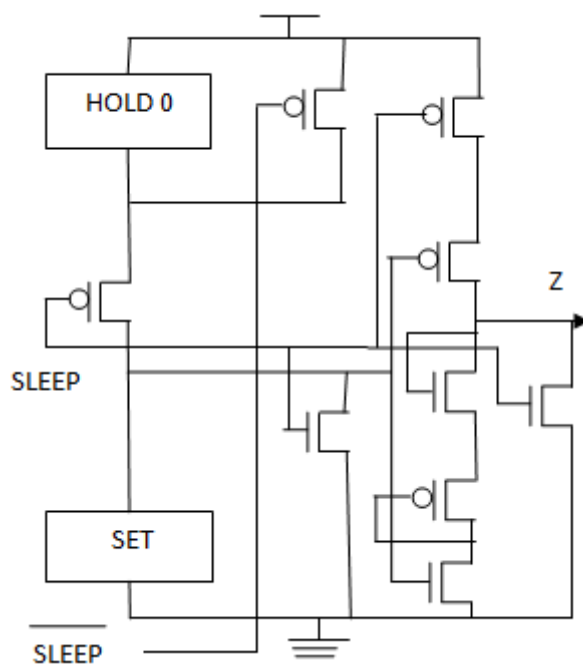
Figure 9 Schematic of Multi Threshold Asynchronous GALEOR Technique

MTNCL+GALEOR technique is competent in idle, active and stand-by modes. It reduces the static leakage power dissipation in idle mode. This proposed method reduces leakage power without increasing switching power.

The Fig. 10 shows the circuit representation of Multi Threshold Asynchronous Galeor based TH22 gate.

It contains hold 0 and set blocks. Boolean expression of this gate is, TH22 = AB whose inputs n=2, threshold of the gate m=2. Here the transistor count seems to be very high and as the transistor count increases, the increases which in turn decreases the power consumption.

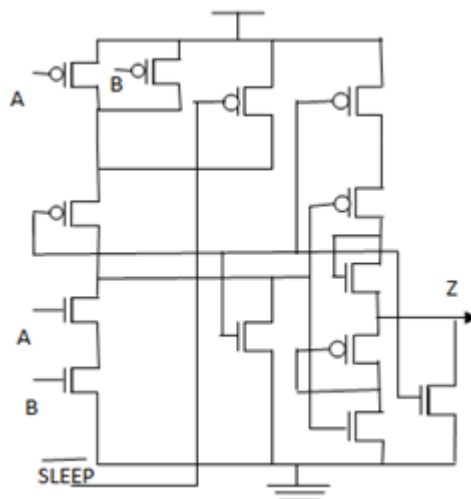**Figure 10** TH22 gate Implementation using Multi Threshold Asynchronous GALEOR

4. SIMULATION AND ANALYSIS

Multi Threshold Null Convention GALEOR technique gives solution to the high performance and low power design requirements of modern VLSI designs. This technique provides the transistors that have low, high and normal voltages. The proposed technique in this paper is schemed for full adder and simulated & functionality vindicated using CMOS technology. High VT & low VT transistors are accustomed in this proposed method to flaunting the rendition benefits and comparison of all the threshold gates. For all the input combinations, the logical functionality of gates is vindicated. The full adder circuit is shown in Fig. 11 with the following functionality.

$$SUM = A \text{ XOR } B \text{ XOR } C$$

$$CARRY = AB + (A \text{ XOR } B) \text{ Cin}$$

For the full adder circuit, sum path is the shortest path and carry path is the longest path in which, low threshold voltage transistors are wonted to demote delay time in the critical path and high threshold voltage transistors are habituated to downgrade power consumption in the shortest path. Power, Slew rate are deliberated for all input combinations during active and idle mode and the delay is analyzed. To compare all the threshold gates of performance matrices, we have performed simulation using Mentor Graphics with umc 130nm technology. The simulation results of full adder are shown in Fig. 12.
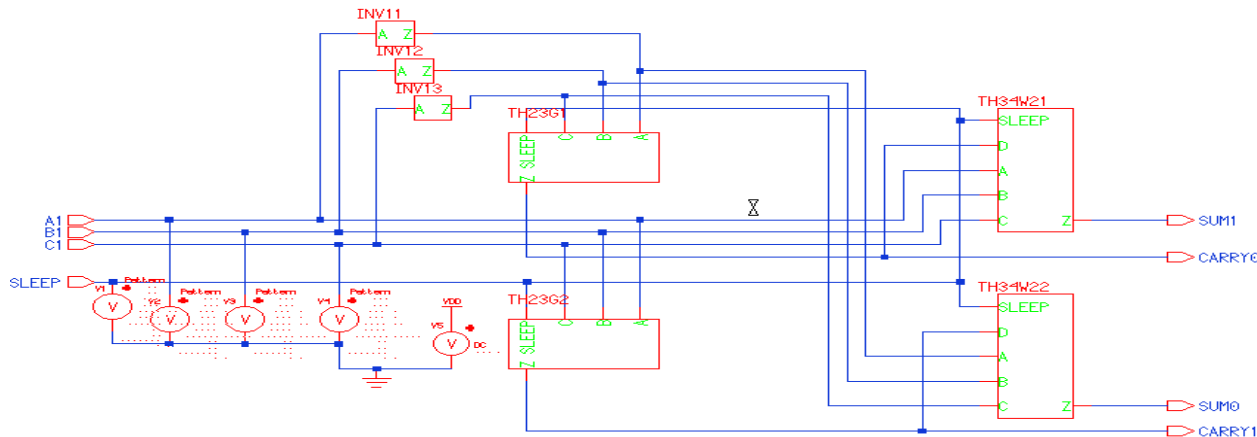
Figure 11 Full Adder Circuit
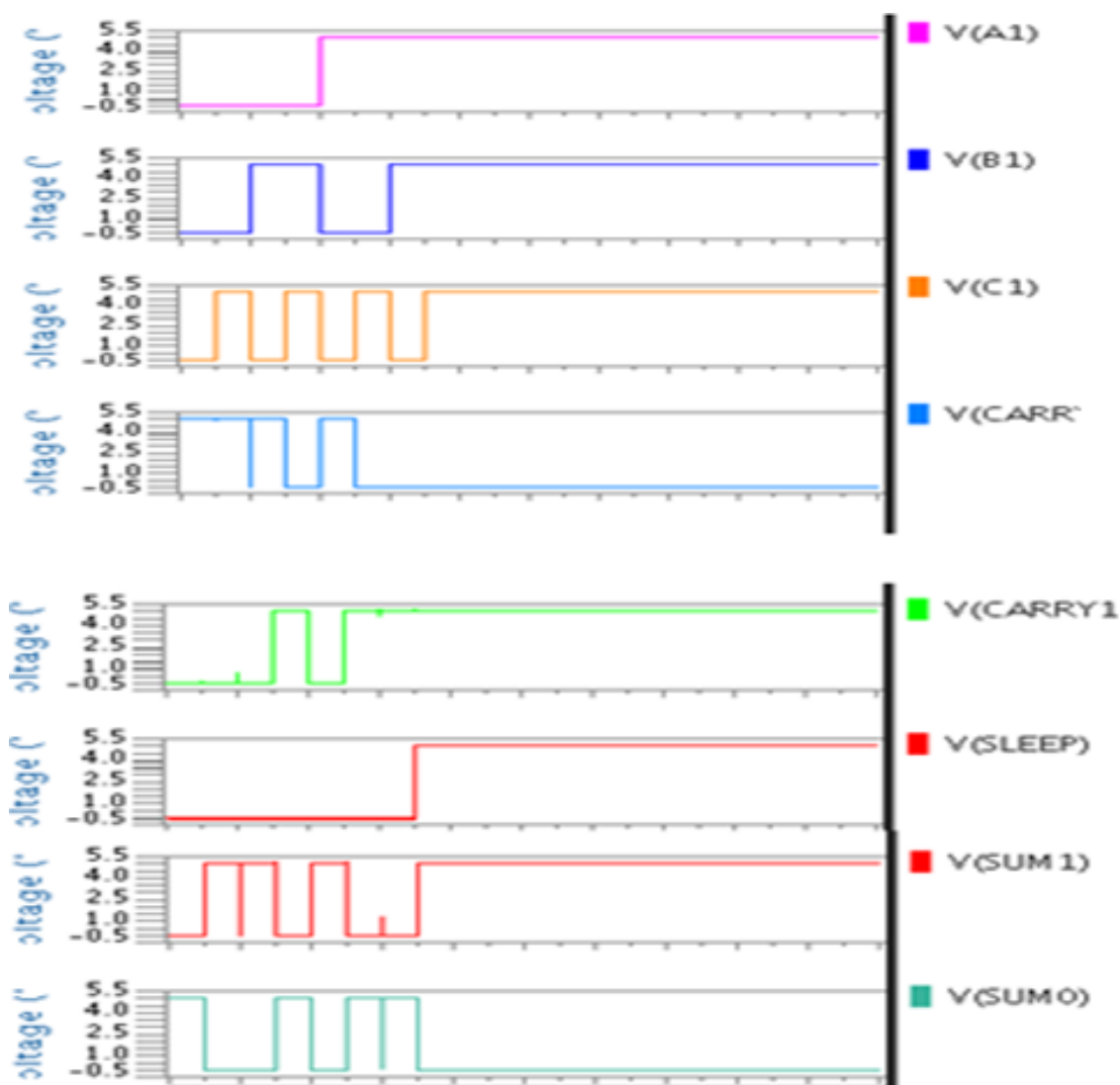
Figure 12 Full Adder Waveforms

Table 1 Comparison Table of MTNCL and Multi Threshold Null Convention GALEOR Techniques

Threshold gates	Power dissipation (n watts)		Delay (ns)		Slew rate(G)		Energy	
	MTNCL	MTNCL+GALEOR	MTNCL	MTNCL+GALEOR	MTNCL	MTNCL+GALEOR	MTNCL	MTNCL+GALEOR
TH12	7.34	4.98	51.61	199.92	23.81	2.07	$1.20×10^{-17}$	$1.5×10^{-14}$
TH22	4.18	3.92	176.19	148.16	16.19	2.43	$7.36×10^{-17}$	$5.80×10^{-17}$
TH13	8.27	5.06	150.06	150.09	29.63	5.64	$1.24×10^{-14}$	$1.20×10^{-14}$
TH23	4.81	3.55	257.50	168.75	19.56	1.95	$1.23×10^{-14}$	$7.67×10^{-17}$
TH33	4.02	3.76	186.28	186.79	19.85	2.94	$3.46×10^{-17}$	$7.02×10^{-17}$

TH23W2	6.39	6.12	149.87	204.79	19.82	3.76	9.57×10^{-17}	1.25×10^{-14}
TH33W2	4.44	4.18	150.13	171.18	21.97	1.98	6.66×10^{-17}	7.15×10^{-17}
TH14	12.64	12.41	349.96	349.96	11.20	2.46	4.42×10^{-14}	4.34×10^{-14}
TH24	15.26	14.35	168.79	267.68	4.28	1.38	2.57×10^{-14}	3.84×10^{-14}
TH34	8.67	8.24	149.06	149.87	12.05	3.47	1.29×10^{-14}	1.23×10^{-14}
TH44	8.94	8.54	98.64	150.97	6.18	1.67	8.81×10^{-17}	1.28×10^{-14}
TH24W2	12.34	12.07	169.58	169.38	16.48	4.79	2.09×10^{-14}	2.04×10^{-14}
TH34W2	4.28	3.94	187.67	169.41	4.28	2.35	8.03×10^{-17}	6.67×10^{-17}
TH44W2	12.05	12.02	148.06	172.94	12.05	2.55	1.78×10^{-14}	2.07×10^{-14}
TH34W3	6.18	5.94	254.84	254.96	6.18	1.37	1.57×10^{-14}	1.51×10^{-14}
TH44W3	16.48	16.07	186.76	186.94	16.48	1.39	3.07×10^{-14}	3.00×10^{-14}
TH24W22	24.25	24.06	154.34	196.34	24.25	6.76	3.74×10^{-14}	4.72×10^{-14}
TH34W22	8.64	8.54	168.34	168.68	8.64	1.97	1.45×10^{-14}	1.44×10^{-14}
TH44W22	22.46	22.04	98.64	138.76	22.46	4.38	2.17×10^{-14}	3.05×10^{-14}
TH54W22	12.34	11.17	184.37	184.96	12.34	2.73	2.27×10^{-14}	2.06×10^{-14}
TH34W32	8.64	7.36	94.49	94.68	8.64	3.47	8.15×10^{-17}	6.96×10^{-17}
TH54W32	4.52	4.06	154.68	168.76	4.52	1.64	6.97×10^{-17}	6.85×10^{-17}
TH44W322	12.36	11.93	198.19	198.37	12.36	3.71	2.45×10^{-14}	2.36×10^{-14}
TH54W322	8.54	8.06	248.67	256.76	8.54	1.44	2.12×10^{-14}	2.04×10^{-14}
THXOR0	4.55	4.28	149.84	149.87	4.55	1.33	6.81×10^{-17}	6.41×10^{-17}
THAND0	4.81	4.54	99.84	99.90	4.81	2.23	4.79×10^{-17}	4.53×10^{-17}
TH24COMP0	4.05	4.28	149.86	149.91	4.05	2.98	6.06×10^{-17}	6.41×10^{-17}
HALF ADDER	32.82	29.84	511.19	99.89	32.85	17.49	16.78×10^{-14}	2.98×10^{-14}
FULL ADDER	39.86	36.68	817.44	149.80	39.86	20.49	32.58×10^{-14}	5.49×10^{-14}
MULTIPLEXER	46.87	44.81	150.76	152.49	41.96	22.67	7.06×10^{-14}	6.52×10^{-14}

Table 1 shows the comparison between MTNCL and our proposed MTNCL+GALEOR techniques. From this table, we observe that proposed technique provides better performance

compared to existing technique. The performance is increased in these parameters power, delay, slew rate & energy. When we consider power consumption parameter, it is high in existing method. It is reduced to 2% in proposed method. The delay is high in existing system; it is reduced in proposed method. However, in the existing method slew rate is low whereas it is high in proposed method. By these parameters, in proposed method the overall energy performance is increased.
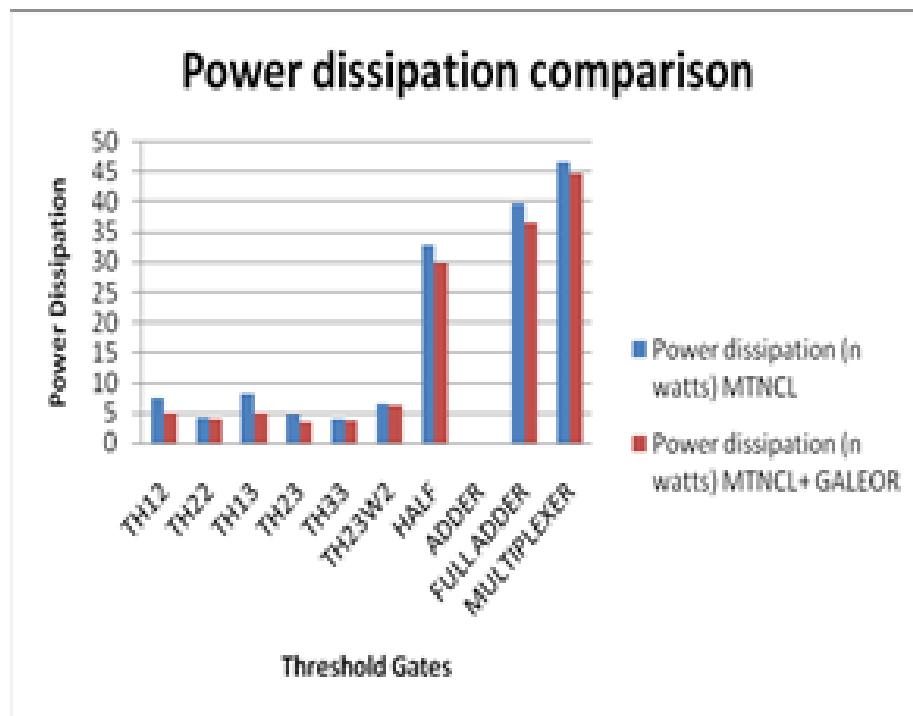

Figure 13 Comparison of Power Dissipation

Power Dissipation is an important aspect in the VLSI circuit design for CMOS technology. Power Dissipation savings of a full adder shown in Fig 13 obtained using Multi Threshold Null Convention Galeor is compared against MTNCL. Proposed method reduces leakage power without increasing switching power. The analysis shows that designs based on Multi threshold asynchronous Galeor gives finer performance compared to MTNCL.

The Gate delay for each logic transition is appraised from 50% of the input voltage swing to that of the output voltage swing. Fig 14 shows the delay comparison between Multi threshold asynchronous Galeor and MTNCL logic gates. Compared to existing methods,
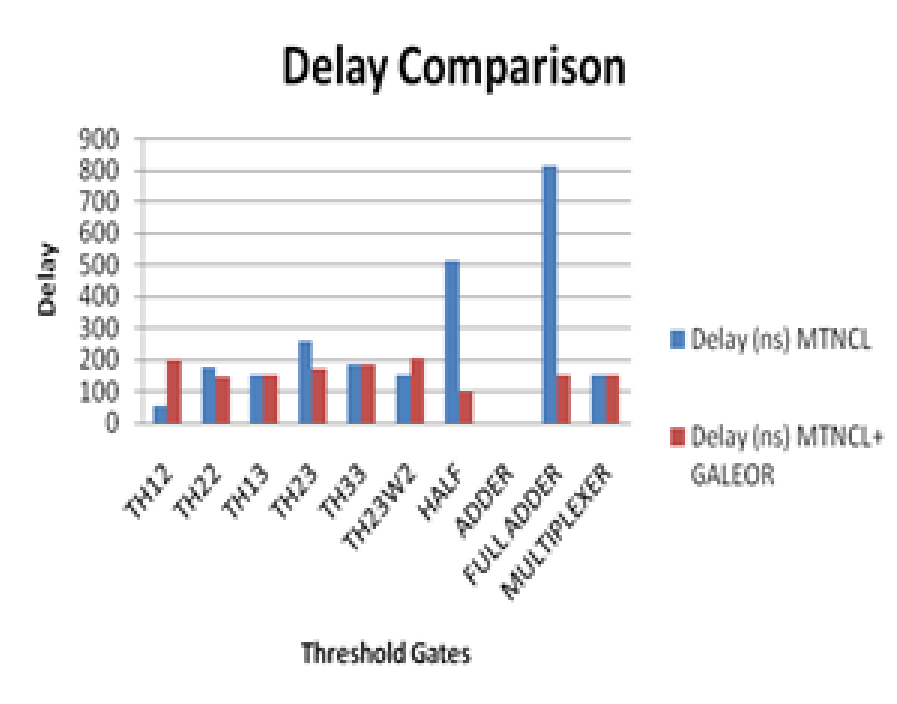
Figure 14 Comparison of Delay

proposed method offers better delay performance.

The rate of change of voltages per unit time is notorious as Slew Rate. The faster response is obtained by high slew rate. From the above figure Fig 15 it is

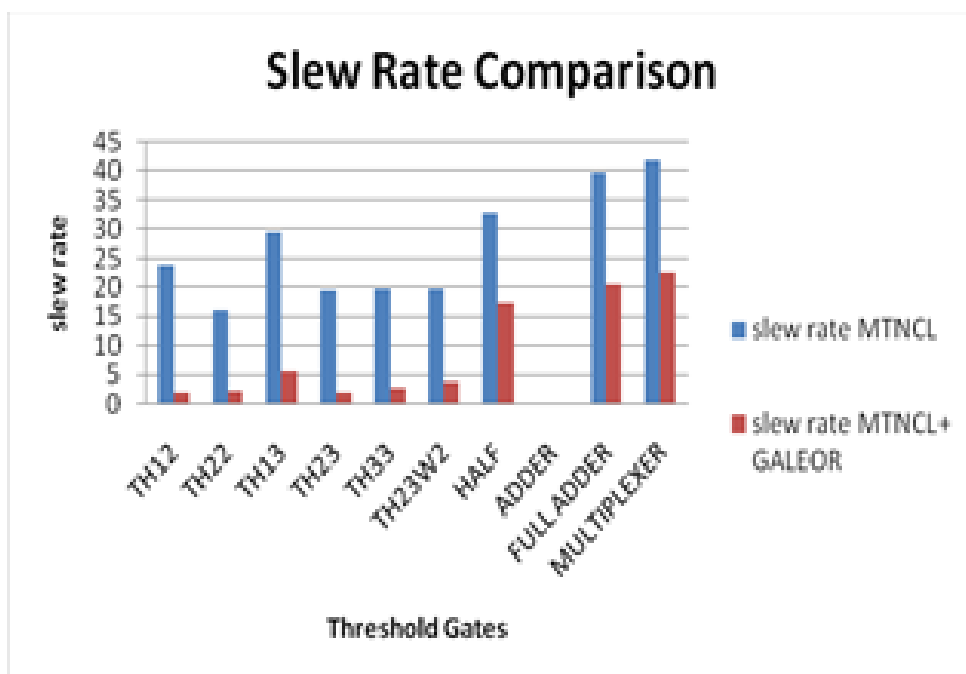It is cleared that proposed technique provides less slew rate compared to MTNCL as shown in Fig 15

Figure 15 Comparison of Slew Rate

5. CONCLUSION

To downgrade power consumption we are having distinct leakage mechanisms. Amid those MTNCL and GALEOR techniques are considered in this paper.

The debit in GALEOR is absence of sleep mode drawbacks and reduces the power dissipation. All the threshold gates are simulated and verified. In this paper, low power, high speed full adder is designed using Multi Threshold Null Convention GALEOR technique. Thus the Multi Threshold Null Convention GALEOR technique provides new methodology for the designers of low power VLSI circuits.

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