International Journal of Trend in Scientific Research and Development (IJTSRD)
International Open Access Journal
ISSN No: 2456 - 6470 | www.ijtsrd.com | Volume - 2 | Issue – 4

# Design of Low Power High Speed D-Latch Using Stacked Inverter and Sleep Transistor at 32nm CMOS Technology

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## ABSTRACT

In this paper we have proposed efficient designs of low power high speed D-latch designed using stacked inverter and sleep transistor based on 32nm CMOS technology. We have designed and simulated these circuits in HSpice simulation tool. In this simulation we have modified W/L ratio of each transistor in the circuit. We have taken power supply of 0.9V. We have calculated average power consumed propagation delay and power delay product.

***Keywords:*** *CMOS, Clock, Latch, Power Delay Product, MOSFET*

## 1. INTRODUCTION

In past few decades an unprecedented growth is experienced by electronics industry and the credit goes to the intelligent use integrated circuits in computation purpose, telecommunications and consumer electronics. We have come a long way since the single transistor era in 1958 to the existing ULSI (Ultra Large Scale Integration) systems with approximately 50 million or more transistors on a single chip. For the modern CMOS features sizes (e.g., 90nm and 65nm), a dominant concern for VLSI circuit designers has become leakage power dissipation. International technology roadmap for semiconductors (ITRS) has reported that leakage power dissipation may dominate total power consumption. Power consumption in CMOS consists of static and dynamic components. Static power is consumed irrespective of transistor switching and dynamic power is consumed while transistors are in switching condition. Dynamic power consumption was earlier (at 0.18μ technology and above) the only major concern for low-power chip designers since it was accounted for more than 90% of the total power supplied to chip. As a result, many earlier proposed techniques, such as frequency and voltage scaling, dedicated on dynamic power reduction. Although, as the feature size reduces, e.g., to 0.09μ and 0.065μ, static power becomes a challenge for current and future technologies.

Designers have limited scope of control. The designer cannot modify the threshold voltage at will. $V_t$ to a high degree or extent is dependent on doping of the substrate material, the thickness of the gate oxide and the potential in the substrate. The physical parameters that cannot be modified by the circuit designer are decided by the process designers are doping in the substrate and the oxide thickness. The designer can willfully vary the substrate potential thereby influencing the $V_t$ via a process known as the body effect. It is risky to tamper with substrate potential, and for digital design the majority connection is invariably shorted to VSS in case of NMOS and VDD in case of PMOS.

As can be seen from the equation, $\boldsymbol{\beta} = \frac{\mu\varepsilon_{ox}}{t_{ox}}\left(\frac{W}{L}\right)$, the designer has no control over the coefficient $\frac{\mu\varepsilon_{ox}}{t_{ox}}$, as the carrier mobility ($\mu_n$ or $\mu_p$) is constant in semiconductor (only influenced by process), $\varepsilon_{ox}$ is a constant physical parameter and $t_{ox}$ is determined by process. Thereby, the designer is left with two dimensional parameters, W and L. In general W and L can be varied together at will by the chip designer, on condition that they remain within the design rule for the minimum dimensions of any feature. Nevertheless with smaller L, the larger is β and lesser the gate capacitance, henceforth the quicker the circuit is, thus with few exceptions designers usually employs the smallest thinkable L available in a process. In conclusion, the lone parameter i.e. the transistor gate width, W, can be controlled at will by the circuit designer and largely the thesis will be concerned with the effect of changing W and arriving at the soundest pick. Hence to get the desired output the width of each MOSFET is modified in all the circuits that have been designed.

## 2. D-Latch

The one-bit digital storage element plays a fundamental role in digital signal processing circuitry. The D-latch whose waveforms are shown in Figure 1 is such a device: it is a memory element having at least two inputs, namely a clock signal {CLK) and a data signal (D) and an output (Q) (and often its complement). The device is ‘transparent' during one of the clock levels the transparent phase during which the output Q follows the input D. But when the clock level is complemented to its isolation phase the logic level present at D is frozen at Q, which remains in that state until CLK returns to its transparent phase. D-latches are categorized as being ‘positive' or ‘negative’, depending upon the logic level of the transparent phase.

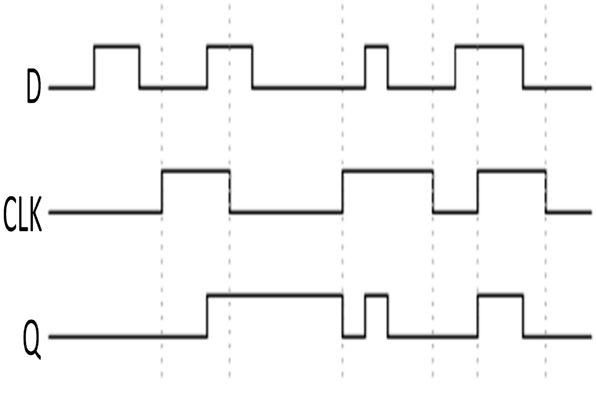

Fig-1: D-latch waveform

## 3. STACKED INVERTER TECHNIQUE

The effect of stacking the transistors may result in the decrease of sub-threshold leakage current while two or more transistors are switched off together. The stacking effect can also be understood from the figure 2 showing forced stack inverter. In the standard inverter there are two transistors only, but in case of forced stack inverter two PMOS pull up transistors and two NMOS pull down transistors are required. All input terminals shares the common input in the forced stack circuit. When the input is ‘0’, then both transistors M1 and M2 are switched off. The $V_x$ is known as the intermediate node voltage here. The transistor M2 has its internal resistance. Due to this internal resistance $V_x$ is more than the ground potential. This positive $V_x$ results in a negative gate to source voltage ($V_{gs}$) for M1 transistor and the negative source to base voltage ($V_{sb}$) for M1. Here M1 has a lessened drain to source voltage ($V_{ds}$), which minimizes the drain induced barrier lowering (DIBL) effect. Altogether these three effects reduce the factor X and henceforth the leakage or static power. All the transistors get the common input therefore this forced stack method is known as a state saving technique.

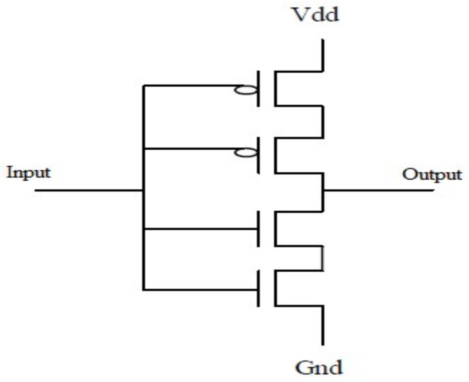

Fig-2: Stacked inverter

## 4. SLEEP TRANSISTOR

State-destructive techniques cut off the transistors (PMOS pull-up or NMOS pull-down or sometimes both) networks from supply voltage or ground by using sleep transistors. These types of methods are also known as gated-GND and gated $V_{dd}$ (Also note that a gated clock is normally used for dynamic power reduction). Mutoh et al. have proposed a technique called as Multi-Threshold Voltage CMOS (MTCMOS), it adds high-$V_{th}$ sleep transistors between PMOS pull-up networks and $V_{dd}$ and between NMOS pull-down networks and GND. The sleep transistors are switched off while the logic circuits are not in usage. By using sleep transistors the logic networks are isolated; the sleep transistor method dramatically lessens leakage or static power during sleep mode. Though, the additional sleep transistors take more area and produce more delay.

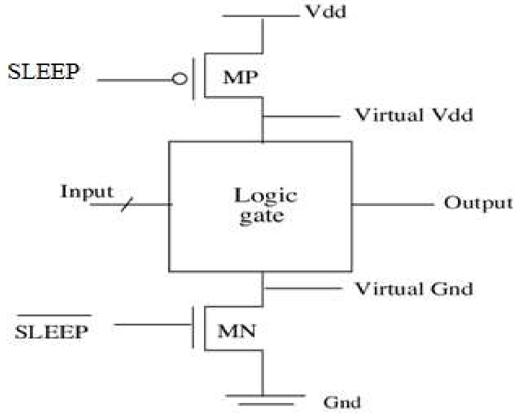

Fig-3: Sleep transistor

## 5. PROPOSED DESIGN USING STACKED INVERTER

We have designed efficient circuit of D-Latch based on stacked inverter using MOSFET which consumes less average power. All circuits are designed using 32nm CMOS technology at 5 GHz. Power supply is 0.9V. Fig. 4 shows circuit diagram of D-latch using stacked inverter.

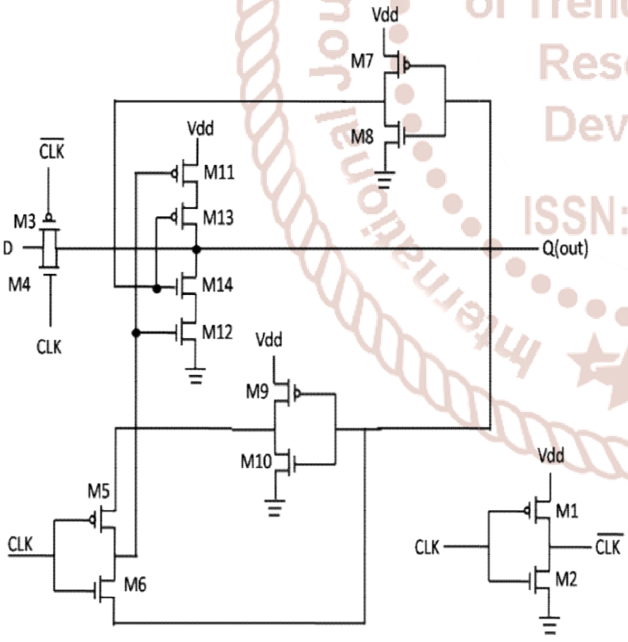

Fig-4: D-latch based on stacked inverter

When clock (CLK) is high, M3, M4 conducts and input D passes to the output. This output also goes to M7, M8, M9, M10 and gets inverted. Now if the clock is low, inverted data switches on M11, M13 (if D = '1') & M12, M14 (if D = '0') and keeps the previous data at the output terminal. This is how the circuit works as a D-latch based on stacked inverter. Table 1 shows the transistors characteristics at 32nm for D-latch design using stacked inverter.

Table 1: MOSFET dimensions for D-Latch based on stacked inverter

| MOSFET | W/L ratio |
|---|---|
| **M1** | 0.563 |
| **M2** | 1.094 |
| **M3** | 0.563 |
| **M4** | 1.094 |
| **M5** | 0.563 |
| **M6** | 0.344 |
| **M7** | 0.469 |
| **M8** | 0.875 |
| **M9** | 0.625 |
| **M10** | 1.000 |
| **M11** | 0.344 |
| **M12** | 0.375 |
| **M13** | 0.438 |
| **M14** | 0.438 |

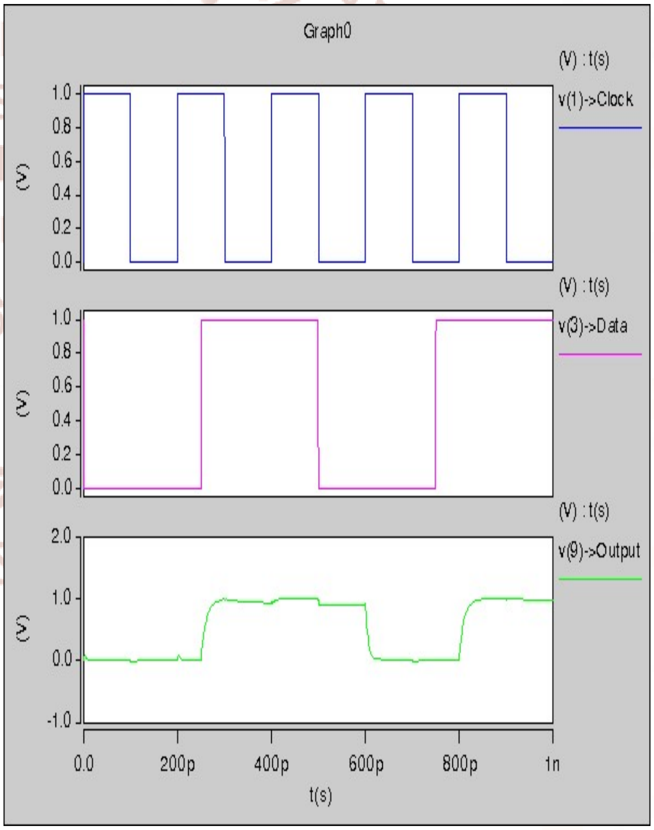

Fig-5: Output for D-latch (stacked inverter)

## 6. PROPOSED DESIGN USING SLEEP TRANSISTOR

We have designed efficient circuit of D-Latch based on sleep transistor using MOSFET which consumes less average power. All circuits are designed using 32nm CMOS technology at 5 GHz. Power supply is 0.9V. Fig. 6 shows circuit diagram of D-latch using sleep transistor.

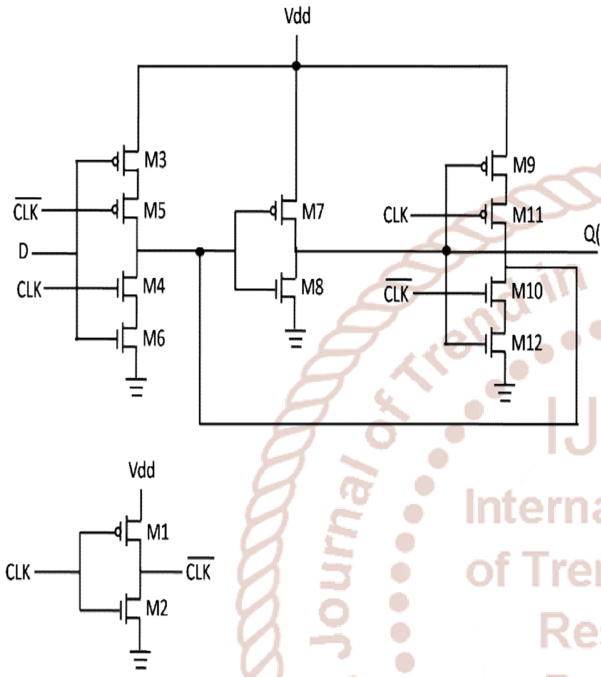

Fig-6: D-atch based on sleep transistor

In this design when clock is high M4, M5 gets ON. If D = ‘0’, logic ‘1’ passes through M3, M5 then gets inverted by M7 & M8 and we get the same data at the output terminal. If D = ‘1’, logic ‘0’ passes through M4, M6 then gets inverted by M7 & M8 and we get the same data at the output terminal. Output data is fed back to M7 & M8 and gets inverted and switches M9 & M12 ON when it is ‘0’ & ‘1’ respectively. Now if the clock is low M11, M10 gets ON and produces previous data at the output terminal. This is how the circuit works as a D-latch based on sleep transistor technique. Table 2 shows the transistors characteristics at 32nm for D-latch (sleep transistor).

Table 2: MOSFET dimensions for D-Latch based on sleep transistor

| MOSFET | W/L ratio |
|---|---|
| **M1** | 0.563 |
| **M2** | 0.406 |
| **M3** | 0.375 |
| **M4** | 0.375 |
| **M5** | 0.438 |
| **M6** | 0.375 |
| **M7** | 0.465 |
| **M8** | 0.563 |
| **M9** | 0.375 |
| **M10** | 0.247 |
| **M11** | 0.543 |
| **M12** | 0.375 |

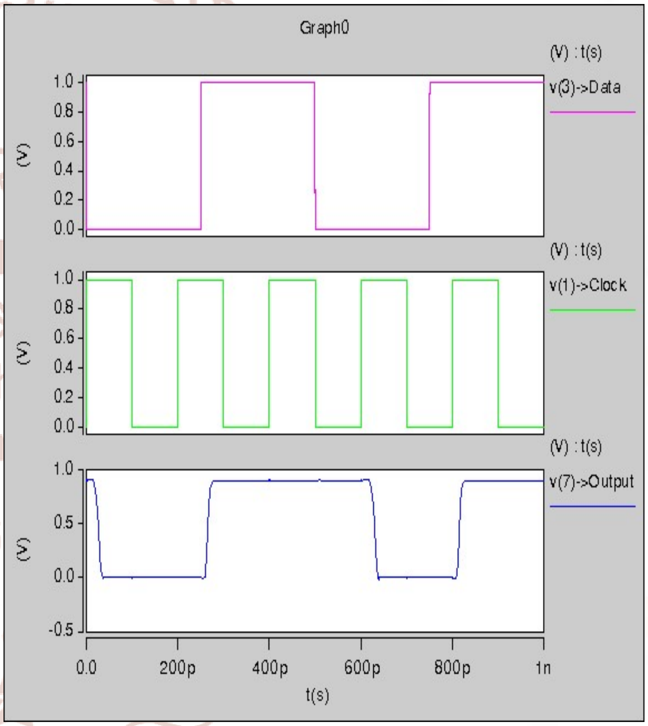

Fig-7: Output for D-latch (sleep transistor)

Table 3 depicts the comparison between these two designs of D-latch according to different parameters.

Table 3: Comparison between designs of D-latch

| Parameters | Stacked Inverter | Sleep Transistor |
|---|---|---|
| No. of transistor | 14 | 12 |
| Average Power (μW) | 0.35 | 0.26 |
| Delay (ps) | 306.04 | 21.5 |
| Power delay product (fJ) | 0.11 | 0.005 |

## 7. CONCLUSIONS

In conclusion, it has been observed that design of D-latch based on sleep transistor shows better performance than stacked inverter. All the simulations are performed n HSpice simulation tool using 32nm CMOS library at power supply of 0.9V for frequency of 5GHz. These designs are working satisfactorily at high frequencies.

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