Designing of IIR Filter using Radix-4 Multiplier by Precharging Technique

Ushanandhini[1], Dr. S. Shivkumar[2]
[1]Research Scholar, [2]Professor
Kalaignar Karunanidhi Institute of Technology, Coimbatore, Tamil Nadu, India

ABSTRACT

Infinite impulse response (IIR) filter designs mainly aims on either low area-cost or high speed or reduced power consumption. Infinite Impulse Response filters are the most important element in signal processing and communication. IIR filters can achieve a given filtering characteristic using less memory and calculations than a similar FIR filter. Multipliers are the basic building block in DSP, microprocessors and other applications. The system's performance is entirely dependent upon the multipliers because they have large area, long latency and consume considerable power hence there is a need to design high speed, low power consumption, regular and less area multipliers. The speed of the multipliers can be increased by reducing the number of partial products. Parallel multipliers are fastest among all multipliers. Booth multipliers are the parallel multipliers that operate on signed operands in two's complement form and have high performance, low power consumption and does not suffer from bad regularity. This paper presents an efficient implementation of high speed parallel multiplier using Radix–4 which further used in the designing of IIR filter. Pre-charging is implemented to increase the lifespan of electronic components and increase reliability of the high voltage system. Pre-charge is intended to minimize propagation delay time. Pre-charge of the power line voltages in a high voltage DC application is a preliminary mode which limits the inrush current during the power up procedure. In other systems such as vehicle applications, pre-charge will occur with each use of the system, multiple times per day.

I. INTRODUCTION

DIGITAL filtering occupies a significant role in digital signal processing and control. However, many applications are beyond the capabilities of conventional digital signal processors. In this context, application specific implementation becomes very attractive. A way to speed up the sampling rate of a filter is to employ fine grain pipelining. This technique is easily applied provided that the system is not recursive. In fact, pipelining such a system has the adverse effect of introducing delays in the feedback loop, which involves latency and negates, therefore, any potential speedup. Recently, two approaches have been proposed to overcome this problem. One of them is the "Scattered Look-Ahead" technique, proposed by Parhi et al. [1]-[3]. It consists of manipulating the transfer function in such a way that a given output value does not depend on the most recent results but rather on previous values computed *n* cycles earlier. A drawback of such an implementation is that the hardware increases with the number of pipelining delays introduced in the feedback loop. It is important to know that the number of pipelining delays increases with the variable precision for a constant sampling rate.

Another group of researchers has observed that the latency in the feedback loop can be kept low, precision independent, provided that the multiplication is carried out most significant digit (MSD) first [4]-[7]. This implies the use of redundant

number systems *[8].* By this way, the latency lies between 2-4 cycles, typically. With such a multiplier, the pipelined recursive filter can easily achieve a high sampling rate, using relatively low hardware. MacNally 's group has recently shown, in implementing a chip, that the second approach combined with the first one requires substantially less hardware than the first one alone, for a given sampling rate [7]. We propose in this paper a systematic procedure for the design of recursive filters. It is based on an algorithm which performs multiplication in MSD first manner [9]-[ll]. It is worth noting that the previous approach consisted mainly in, first constructing a multiplier by properly assembling its components, and then realizing the filter. It is clear, with this approach, that the characteristics and performance of the filter depend highly on those of the multiplier. In contrast, with our approach the characteristics are decided rather at the algorithm level, by properly determining the parameters of the algorithm. In this way, the multiplier is realized according to the filter to be implemented, not the opposite. This insures the best performance and the minimum hardware. Our approach is flexible enough to choose freely the number system radix. Then, it would be more profitable to adopt a radix-4 representation rather than a radix-2 to generate half the number of partial products, which requires about half the hardware. Furthermore, our approach allows us to interleave easily two multiplier arrays into one. In this way, long interconnections are avoided and a denser and more regular layout is achieved. With such an array a second order all-pole filter is realized in this paper, operating in radix-4 representation and implemented with only one array. The organization of the paper is as follows. Section II is devoted to the development of two devices using redundant arithmetic. These devices are needed for the realization of the algorithm which is presented in Section III. Then, the realization of the second order all-pole filter is shown in Section IV. The discussion and conclusion are found in Sections V and VI, respectively.

II. LITERATURE REVIEW

This review literature contains a brief description of the ways in which the iir filter using radix-4 multiplier various fields and various techniques of digital communication system. The use of low power hybrid polyphase filter in BFSK receiver to achieve a high frequency offset tolerance at a low MI is demonstrated in research paper [2]. The above is achieved by frequency to energy conversion of data samples using PPFs architecture. However, PPFs were originally utilized to reject image signals in low-IF receivers and also as a demodulator in a zero-IF BFSK receiver but extra filters were required for channel selection and interference rejection. This paper [3] addresses this issue from the perspective of minimizing the total power consumption of a mobile terminal while maintaining a guaranteed quality-of-service (QoS). However, due to the integration of multimedia services, the escalating energy consumption of a mobile unit is also becoming a dominant factor in the design of communication systems. Also, two technologies have been described in this paper that can make a wireless multimedia communication system more energy efficient while ensuring quality-of-service.

As a second application, RS codes have been merged with OFDM modulators, leading to a novel transmission scheme, called RS-OFDM, in which part of the RS code contributes to the OFDM modulator. Both applications rely extensively on the critically sub-sampled filter bank representation of RS codes. Multirate filters have been design using SDR concept in paper [12]. Two SDR models are considered; one with system generator and one which was based on MATLAB Simulink. The results show that both models can produce the desired audio sample rate. The main advantage of using SDR concept is; processing can be done at any sampling rate within a wide range of rates. It has some limitation; both models are operated at different sampling rates. This paper [13] provides the design and implementation of high speed CIC decimator for wireless applications like GSM. It reduces the need for expensive anti-aliasing analog filters. It provides enhanced performance in terms of speed and area utilization. However, the frequency response is not accurate. Research Paper [14] performed the results of a comparison of different decimation architectures for high resolution sigma delta analogue to digital conversion in terms of pass band, transition band performance, simulated signal to noise ratio, and computational cost. They provide excellent comparison of the different IIR filters for low group delay audio applications. This is the main benefit. But they provide only theoretical overview of different IIR filters. An interpolator has been designed in research paper [15] and simulated by using direct form polyphase serial and parallel structures to reduce area and to enhance speed. However, the result shows

that serial interpolator can enhance speed by 5.6% as compared to MAC based design. On the other hand, they required more hardware. Research paper [16] develops a IIR digital filter design for the vestigial side band (VSB) modulator required in the analog TV transmission systems, like PAL. The main benefit of it is that the resulting design has significantly lower complexity than in the earlier designs using FIR filters and it is quite feasible for implementation as an ASIC or even on an FPGA circuit. However to avoid overflow and to satisfy round-off noise requirements, three more additional bits are required, which is its major limitation. This paper [17] describes the use of a polyphase IIR filter bank to perform the interpolations required for symbol timing synchronization in a sampled- data receiver. Maximum likelihood timing synchronization techniques can be easily incorporated into the polyphase filter bank in a natural way. Advantage of it is that; separate interpolating filter following the matched filter is not required. It has some limitation also; necessary of auxiliary control to adjust the clocking of data into the filter bank for small differences in the sample clock and data clock. In [18-21] throughputs with code-division multiplexing (CDM) and time-division multiplexing (TDM) for downlink packet transmission in IIR based code-division multiple access (CDMA) systems has been compared. Also, propose and use a model that can show the impact of self-interference on the received bit energy per noise and interference power density. A generic performance analysis for the IIR and variable spreading factor (VSF) IIR schemes in a multicarrier code division multiple accesses (MCCDMA) system is presented. Moreover, the analysis takes into account the inter symbol interference (ISI) caused by the multipath delay components exceeding the guard interval, which is usually omitted in the literature. It examines erasure resilience of oversampled filter bank (OFB) codes, focusing on two families of codes based on cosine modulated filter banks (CMFB). The most computationally intensive part of a wideband receiver is the channelizer. However, the computational complexity of linear phase finite impulse response (LPFIR) filters employed in the channelizer is dominated by the number of adders used in the implementation of the multipliers. In this paper [22-23], two methods are proposed to efficiently implement the channel filters in a wideband receiver based on common sub expression elimination (CSE). It is concerned with communicating parallel independent streams of data, probably of different

rates, through a multiple-input multiple-output channel. Each data stream is essential to satisfy a bit-error-rate (BER) constraint. Moreover, multicarrier code-division multiple access (MC-CDMA) is a promising candidate for the air interface of future wireless communication systems. In paper [24], a novel space-frequency multiuser detection scheme for IIR filter uplink MC-CDMA systems with multiple receive antennas has been proposed. The most computationally demanding block in the digital front end of a software defined radio (SDR) receiver is the channelizer which operates at the highest sampling rate. Reconfigurability and low complexity are the two key requirements of the SDR channelizers. Architecture for implementing low complexity and reconfigurable finite impulse response (FIR) filters for channelizers is proposed in paper [25]. Research paper [26-27] introduced the rate distortion optimized resource allocation for video transmission over IIR wireless direct-sequence code-division multiple-access (DSCDMA) channels. Also, consider the performance of transmitting scalable video over a multipath Rayleigh fading channel via a combination of multi-code IIR CDMA and variable sequence length IIR CDMA channel system. This paper [28] presents a dual-mode Residue Number System (RNS) based decimation filter which can be programmed for WCDMA and 802.16e standards. Decimation is done by using multistage, IIR finite impulse response (FIR) filters. These filters are implemented in RNS domain offers high speed because of its carry free operation on smaller residues in parallel channels. In [29-31] the invertibility of M-variate polynomial (respectively: Laurent polynomial) matrices of size N by P has been studied. Such matrices represent multidimensional systems in various settings including filter banks, IIR systems and multiple input multiple-output systems. QoS routing in multi-channel wireless mesh networks (WMNs) with contention-based MAC protocols is a very challenging problem. To cope with the problem, a rate-loss function, has been proposed in [32], which is a quantitative metric used to evaluate how critical the performance anomaly problem occurred in each orthogonal channel. In addition, a distributed Rate-Loss based Channel Assignment (RL-CA), has been presented, which enables each router to select channels suffering from the slightest performance anomaly problem in a distributed manner. With the hasty growth of internet contact and voice and information centric communications, many contact technologies have been urbanized to meet the stringent insist of high speed information transmission

and viaduct the wide bandwidth gap among ever-increasing high data- rate core system and bandwidth-hungry end-user complex. Advancements of IIR indication processing methodologies have been introduced in [33] that are aggravated by this design trend. Applications of IIR digital filters in DS/CDMA code acquisition, Kalman filtering for optimal signal reconstruction from noisy sub-band system and lossy compression approach to Tran's multiplexed images are also reviewed. IIR based Pulse Shaping Filters or Root Raised Cosine (RRC) low pass filters emerges as one of the hottest topic in field of wireless communication technology [34]. Low pass filters are used for decimation and for interpolation. When decimating phenomenon occurs, low pass filters are used to reduce the bandwidth of a signal prior to reducing the sampling rate. This is done to diminish aliasing due to the reduction in the sampling rate. While interpolating, low pass filters are used to remove spectral images from the low-rate signal. In paper [35], area efficient and cost effective techniques for design of pulse shaping filters have been presented to improve the computational and implementation complexity. In paper [35] a method has been proposed to realize low complexity reconfigurable channel filters based on decimation, interpolation and masking techniques. Moreover, the enhancement in center frequency resolution and the increased number of channel filter frequency responses are obtained without any hardware overhead. During the last several years there has been substantial progress in IIR filter system research. However, this includes design of decimation and interpolation filters, analysis or synthesis filter banks also called quadrature mirror filters, or QMFJ, and the enlargement of new sampling theorems. Polyphase filters are becoming a very important component in the design of various filter structures due to the fact that it reduces the cost and complexity of the filter by doing the process of decimation prior to filtering which reduces the multiplications per input sample. In paper [38] a basic polyphase filter and its applications have been reviewed. The design and simulation of multi rate decimation filter to work with wireless mobile system under software defined radio (SDR) technology have been described in [39]. In [40] a low-complexity IIR filter 3-D spatio-temporal FIR cone and frustum filter structure is proposed having potential applications as a spatio-temporal directional filter. The cone filter structure utilizes a 1-D modified discrete fourier transform (DFT) filter bank and 2-D spatial filters. The frustum filter along with a double-frustum-shaped

pass band oriented along the temporal frequency axis is approximated by employing an appropriate subset of sub bands. Moreover, Low computational complexity is achieved by maximal decimation in the temporal dimension and by employing the IIR filter using radix-4 multiplier by pre-charging technique.

III. SYSTEM DESIGN

The objective of the most IIR coefficient calculation methods is to obtain values of h (n) such that the resulting filter meets the design specification and to find whether it is possible to design filter with such specifications such as amplitude, frequency, response and throughput requirements. Several methods are available for obtaining h(n). The impulse invariance, optimal and bilinear transformation method are the most commonly used. We have used mat lab for checking the filter specifications. Although the above requirements are application dependent it will be helpful to devote some time on the characteristics of the filter. The characteristics of the filter are generally specified in frequency domain. For frequency selective filters, such as low pass and band pass filters. The IIR filter specifications are generally represented in terms of tolerance. The Digital IIR Filter Design problem involves the determination of a set of filter coefficients to meet a set of design specifications. These specifications typically consist of the width of the pass band and the corresponding gain, the width of the stop band(s) and the attenuation therein; the band edge frequencies (which give an indication of the transition band) and the peak ripple tolerable in the pass band and stop band(s). In the pass band, the magnitude response has a peak deviation of and in the stop band, it is maximum deviation of a. The width of transition band determines how sharp the filter is. The magnitude response decreases monotonically from the pass band to stop band in this region.

The functional requirement of the high voltage pre-charge circuit is to minimize the peak current out from the power source by slowing down the dV/dT of the input power voltage such that a new "pre-charge mode" is created. Of course, the inductive loads on the distribution system must be switched off during the pre-charge mode. While pre-charging, the system voltage will rise slowly and controllably with power-up current never exceeding the maximum allowed. As the circuit voltage approaches near steady state, then the pre-charge function is complete. Normal operation of a pre-charge circuit is to terminate pre-charge mode

when the circuit voltage is 90% or 95% of the operating voltage.

A. PRECHARGE

Pre-charge is intended to minimize propagation delay time. Pre-charge of the power-line voltages in a high voltage DC application is a preliminary mode which limits the inrush current during the power up procedure. A high-voltage system with a large capacitive load can be exposed to high electric current during initial turn-on. This current, if not limited, can cause considerable stress or damage to the system components. In some applications, the occasion to activate the system is a rare occurrence, such as in commercial utility power distribution. In other systems such as vehicle applications, pre-charge will occur with each use of the system, multiple times per day. Pre-charging is implemented to increase the lifespan of electronic components and increase reliability of the high voltage system.

B. IIR FILTER

IIR filters are one of two primary types of digital filters used in Digital Signal Processing (DSP) applications (the other type being FIR). IIR filters are digital filters with infinite impulse response. "IIR" means Infinite Impulse Response". Unlike FIR filters, they have the feedback (a recursive part of a filter) and are known as recursive digital filters therefore. For this reason, IIR filters have much better frequency response than FIR filters of the same order.
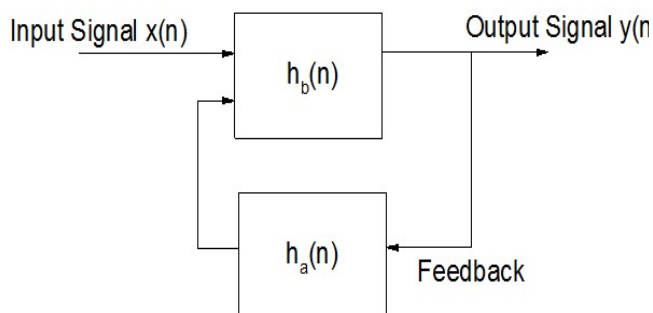
Fig: 1 Block Diagram for IIR filter

In this case the filter output depends upon previous inputs, present inputs and also on previous outputs. IIR filters are useful for high-speed designs because they typically require a lower number of multiply compared to FIR filters. IIR filters can be designed to have a frequency response that is a discrete version of the frequency response of an analog filter. These filters also are very sensitive to filter coefficient

quantization errors that occur due to using a finite number of bits to represent the filter coefficients.

C. RADIX-4 MULTIPLIERS

Booth algorithm is a powerful algorithm for signed number multiplication, which treats both positive and negative numbers uniformly. Since a k-bit binary number can be interpreted as k/2-digit Radix-4 number, a k/3-digit Radix-8 number and so on, it can deal with more than one bit of the multiplier in each cycle by using high radix multiplication. The major disadvantage of the Radix-2 algorithm was that the process required n shifts and an average of n/2 additions for an n bit multiplier. This variable number of shift and add operations is inconvenient for designing parallel multipliers. The Radix-2 algorithm becomes inefficient when there are isolated 1's. The Radix-4 modified Booth algorithm overcomes all these limitations of Radix-2 algorithm. For operands equal to or greater than 16 bits, the modified Radix-4 Booth algorithm has been widely used. It is based on encoding the two's complement multiplier in order to reduce the number of partial products to be added to n/2 .

IV. RESULT AND DISCUSSION

This chapter shows the simulation output results of the proposed system that had been designed using Xilinx tool output waveforms for the simulation results for given input signal. Up to now, we have described in detail the design procedure by using an example. In this section the general character of the procedure is emphasized. We can see, in this way, Its systematic nature in a more noticeable way. This makes easier the possibility of applying the design procedure to other types of problems involving multiplications. For completeness, this section ends with the evaluation of the complexity and performance of the filter realized in this paper.
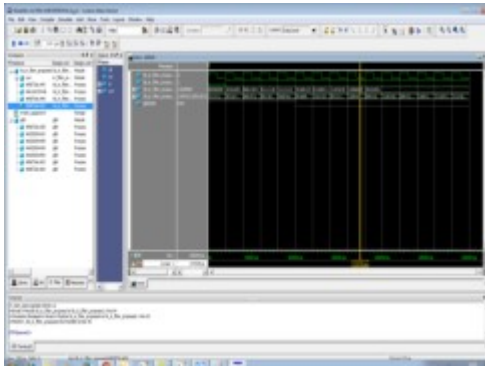
Fig: 2 IIR filter with normal multiplier – decimal and RTL schematic

Due to its regular structure, the proposed multiplier was implemented in VHDL for arbitrary word sizes *M* and *N* and optional pipelining using VHDL generate statements and Xilinx primitives. It can be observed that the proposed IIR filter design describe clearly outperforms all previous multipliers for any input size various bit in terms of slice usage, Table 1 described the existing multiplier and proposed multiplier design compression results ,the result shows the proposed one is better than previous existing result.

Parameter	Existing–multiplier	Multiplier with DRP Technique
Slice LUTs	64	64
BELS	126	128
Combinational Delay	29.558ns	22.562ns

Table 1: Comparison table of Booth Multiplier with Existing method and with proposed DRP Technique

The below table shows parameter comparison about area and delay between the existing system and with the existing system with DRP Technique. Thus the area and delay is reduced more by DRP Technique when compared to the existing system without DRP Technique.

The below table shows parameter comparison of IIR filter about area, delay, frequency, power and throughput between the existing system and with the existing system with DRP Technique.

Finally result shows table 2 explained existing power 96.97 Mw and proposed system power consumption is 33.59 Mw only less than half that is 1:3 amount of power consumed proposed system, combinational delay frequency, delay, BELS, sliceLUTs, throughput values are better result compared to existing result,

each system same input value but result obtained better result for other existing system, proposed multiplier with DRP techniques given better result for other.

Parameter	IIR – Existing –Multiplier	IIR - multiplier with DRP Technique
Slice LUTs	186	188
BELS	543	546
Delay	15.008ns	12.236ns
Combinational Delay	33.086ns	25.826ns
Frequency	66.631MHz	81.726MHz
Power	96.97mW	33.59mW
Throughput	1066 Mbps	1307 Mbps

Table 2: Comparison table of IIR Filter with Existing method and with proposed DRP Technique

V. CONCLUSION

Thus IIR Filter is designed and DRP Technique is implemented. By simulation process using Xilinx Tool, the outputs are obtained. The results shows that, the proposed system has reduced area, power, throughput, frequency levels and delay than existing system. Because When the entire NOT gates in Ex-or gates are replaced by Ex-or gates itself, it results in Good (Higher) performance of the system. Instead of using IIR filter, FIR filter is replaced and the same process is carried out. Based on the results among these two filters, the efficient filter is chosen. In future, a detailed Research Study about reduction in area, power and delay using various Simulation Tools is done.

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