



## Optimized Carry Speculative Adder

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### ABSTRACT

Arithmetic logic units and digital signal processors widely uses adders. It is the most complicated arithmetic circuits in digital electronics. The existing adders suffer from critical path delay, area overhead and power consumption. Speculative adders are designed with variable latency that combines speculation technique along with correction methodology to attain high performance in terms of low area overhead over the existing adders. In speculative adders the sum and carry generation part is separated to reduce the area overhead. Carry Speculative Adder (CSPA) uses carry predictor circuit to reduce power consumption and to reduce the computational time and it uses error recognition and error correction circuit to find the fault occurred in the partial sum generator and to recover it to get accurate results.

**Keywords:** Arithmetic logic units(ALUs), Digital Signal Processors(DSPs), Carry Speculative Adder (CSPA)

### I. INTRODUCTION

Circuit delay plays a key role in any system particularly in Adders. Addition is a crucial arithmetic operation because it usually involves a carry ripple which propagates from each bit to its next higher bit position. This results in a substantial circuit delay. Their throughput affects the overall performance of the system. Traditional n-bit adders provide accurate results, but the lower bound of their critical path delay is  $\Omega(\log n)$  i.e., logarithmic delay that is long delay and requires large power consumption. There is always a trade-off between Area, Power and Delay.

Any changes made to one parameter may affect any other two parameters. Approximation can increase performance or reduces power consumption with a simplified or inaccurate circuit by sacrificing output.

In this, Carry Speculative Adder Using Modified Carry Generators is proposed which generates sub logarithmic delay with less area and delay and also implementing with variable latency, which gives same results similar former adder and can be used in DSP Applications.

### II. METHODOLOGY

Carry Speculative Adder (CSPA) is used to reduce the critical path delay of the circuit. It is based on carry speculation. The block diagram of the carry speculative adder (CSPA) is shown in figure 2.1

The n-bit Carry Speculative Adder is divided into several small blocks adders and Carry Predictor Circuits that are operated independently. Except for the leftmost block adder, the size of each block adder size is x. Number of block adders is represented as 'm'.

Therefore, There are 'm' independent block adders and '(m - 1)' carry predictor circuits in a Carry Speculative Adder. The value of m is given as by equation 2.1.

$$m = (n/x) \dots\dots\dots 1.1$$

**Table 1: Truth Table of Carry out Signal in Traditional Full Adder**

C <sub>IN</sub>	A	B	C <sub>OUT</sub>
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

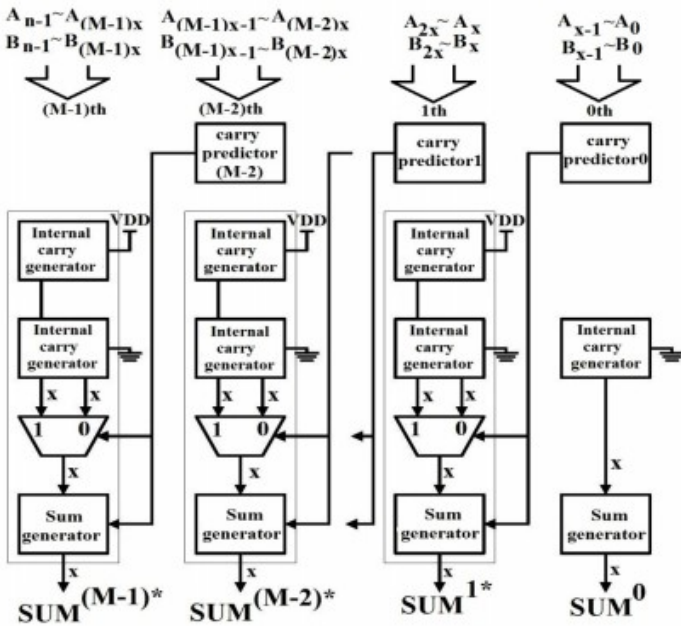


Fig 2.1: Block diagram of carry speculative adder

**III. DETAILED DESIGN**

**Modified Carry Generators:**

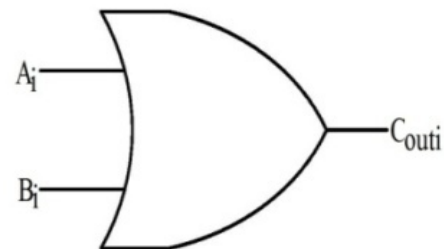
In Carry Speculative Adder, the Block Adder is implemented with Modified Full Adder. It separates Carry Generator and Sum Generator to produce carry output and sum out outputs with an extra logic gate which leads to increase in power consumption and area increase. To reduce the area and improve performance of adder, these carry generators in block adder of Carry Speculative Adder are replaced by using two separate carry generators for inputs C<sub>in</sub>=1 and C<sub>in</sub>=0 respectively. In Traditional Full Adder, the carry out signal equation is given by equation 3.1. Using logic complexity reduction, the Carryout signal equation is simplified to equation 3.2 and equation 3.3 as follows. The truth table of carry generator and modified carry generators is shown below.

- COUT= A.B+B.C+C.A ..... 3.1
- When C<sub>in</sub>=0, COUT= A.B ..... 3.2
- When C<sub>in</sub>=1, COUT= A+B ..... 3.3

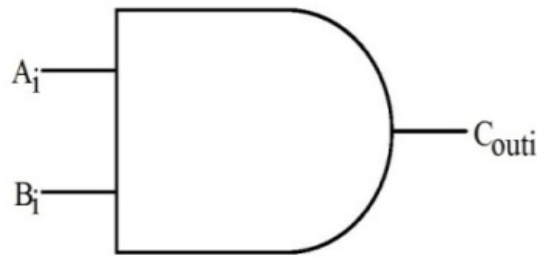
**Table 2: Truth Table of Modified Carry Generators**

When C <sub>in</sub> =0			When C <sub>in</sub> =1		
A	B	C <sub>OUT</sub>	A	B	C <sub>OUT</sub>
0	0	0	0	0	0
0	0	0	0	1	1
1	0	0	1	0	1
1	1	1	1	1	1

The block diagrams of carry generators are shown in figure 3.1 and figure 3.2. When carry in input of block adder is logic one, the carry generator is replaced with logic OR gate and when carry in input of block adder is logic zero, the carry generator is replaced with logic AND gate respectively. Thus in block adders, instead of two carry generators, two types of modified carry generators are used to implement the block adder of Carry Speculative Adder which provides one gate delay with reduced area. These carry generators generate Carry's simultaneously without using C<sub>in</sub> bit.



**Figure 3.1: Block Diagram of Modified Carry Generator for C<sub>in</sub>=1**



**Figure 3.2: Block Diagram of Modified Carry Generator for  $C_{in}=0$**

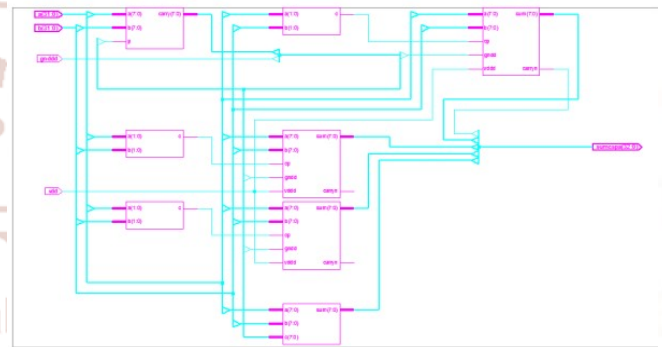
Adder using Modified Carry Generators. When an error is occurred, the input registers in the Variable Latency Carry Speculative Adder using Modified Carry Generators (VLCSPPAM) are disabled and no new input is latched in the circuit. Hence to get continuous data in the circuit, a data latching circuit which consists of Xor gate is replace in place of not gate. In the latching circuit, an exclusive or operation is performed between Error signal and complement of Error signal. The output of data latching circuit valid enables to latch new data into input registers after the old data is recovered.

**IV. VARIABLE LATENCY CARRY SPECULATIVE ADDER USING MODIFIED CARRY GENERATORS**

In Variable Latency Carry Speculative Adder using Modified Carry Generators (VLCSPPAM), Carry Speculative Adder using Modified Carry Generators is added with Error detection circuit, Error recovery circuit, Data latching circuit and multi-bit multiplexor as shown in figure 4.1. When an input pattern is arrived, Variable Latency Carry Speculative Adders using Modified Carry Generators gives the result of the Carry Speculative Adder using Modified Carry Generators (i.e., SUM\*) in a one cycle. The error detection circuit determines whether an error has occurred or not and also indicates which block adder produces the incorrect partial sum and correct partial sum.

**A. RESULTS**

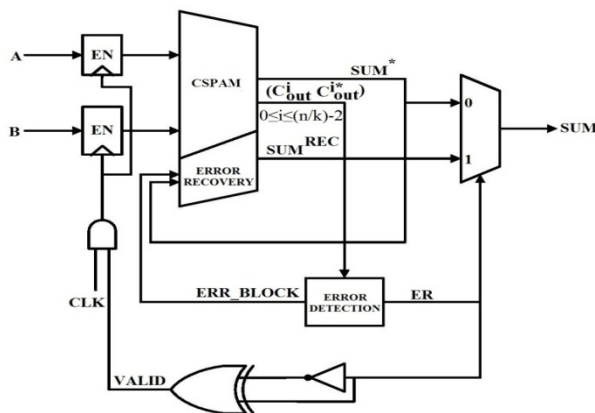
*RTL schematic of existing technique:*



*Simulation results of Carry Speculative Adder:*

Here, the size of the Carry Speculative Adder is 32 bit; length of each block adder is 12 bit and number of block adders is equal to 3. Here the signal VCC is set at high and GND is set at low.

The input A is given as “0000 0000 0000 0001 1110 0110 0110 1011” which equal to “255595” in decimal and input B is given as “0000 000 0010 0011 0101 1000 1110 1011” which equal to “2316523” in decimal. The sum of the two numbers in normal addition process is “2572118”.



**Figure 4.1: Variable Latency Carry Speculative Adder using Modified Carry Generators**

The error recovery circuit recovers the results when an error occurs based on the ERR\_block in the next clock cycle. The results from error recovery circuit and Carry Speculative Adder using Modified Carry Generators are given to multi-bit multiplexor and the error is used as multiplexor select signal to select one of the sum results. When the ER signal is “1”, the multiplexor selects recovers signal from error recovery circuit. When the ER signal is “0”, the multiplexor selects results from Carry Speculative

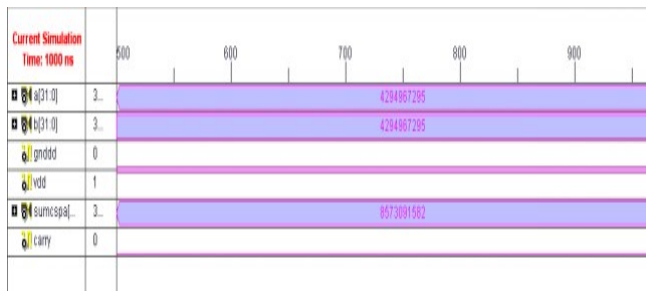
Current Simulation Time: 1000 ns	500	600	700	800	900
q[31:0]	3.			4294867295	
q[31:0]	3.			4294867295	
g[0:0]	0				
v[0]	1				
sumspec[31:0]	3.			8573891582	
carry	0				

*Simulation Results for Carry Speculative Adder using Modified Carry Generators:*

Figure below shows the simulation results of Carry Speculative Adder using Modified Carry Generators. Here, the size of the Carry Speculative Adder using

Modified Carry Generators is 32 bit; length of each block adder is 12 bit and number of block adders is equal to 3. Here the signal VCC is set at high and GND is set at low.

The input A is given as "0000 0000 0000 0001 1110 0110 0110 1011" which equal to "255595" in decimal and input B is given as "0000 000 0010 0011 0101 1000 1110 1011" which equal to "2316523" in decimal. The sum of the two numbers in normal addition process is "2572118".



## CONCLUSION:

Carry Speculative Adder using Modified Carry Generators uses separate carry generators circuits to generate carry signals with less number of gates compared to traditional full adder. Carry Speculative Adder using Modified Carry Generators improves the performance of the adder and reduces the area producing accurate results. Carry Speculative Adder using Modified Carry Generators is also implemented with variable latency design to produce accurate results.

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