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Area Efficient Full Subtractor Based on Static 125nm CMOS Technology

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ABSTRACT
A combinational logic circuit is said to be independent of time since it gives the results based on present input not past input. This research is concerned about the comparison between currently existing full subtractor IC and the subtractor which is built efficiently in the 125nm and observing the distortion and changes caused in the result of both full subtractor. The behaviour of the efficient full subtractor is designed using tanner eda tools which was useful and the currently existing full subtractor is designed using xilnx software and lastly the layout for this research is designed with the help of multisim. With help of this research many newly created circuits can designed much more smaller.

Keyword: *Full Subtractor, cmos, static CMOS, 125nm, tanner, multisim, Xilinx, half subtractor*

I. INTRODUCTION

a logic gate is a physical device implementing a Boolean expression that is, it performs a logical design operation on one or more binary inputs and produces a single binary output. In digital circuit theory, combinational circuits which is also called as time independent logic is a type of digital logic which is implemented by Boolean circuits in which the output is the pure function of the input. has reduced propagation delay and it has faster addition logic. A full subtractor is a combinational logical design that performs subtraction of two binary bits, one is said to be minuend and other is subtrahend, borrow of the previous adjacent lower is minuend bit. This circuit has three inputs and two outputs. The inputs ‘a’, ‘b’ and ‘c’, denote the minuend, subtrahend, and previous borrow, respectively. The outputs, Difference and Borrow represent the difference and outputs borrow, respectively. Subtractor and adders are used in almost all integrated circuits. as for now adders and subtractors are used for education purpose but in order check a ouput of the full subtractor a student has to connect multiple gates . If all the required gate are integrated into a single chip .It will be easy to analyze the circuit very fastly and accurately. The Full subtractor constructed in this research paper is constructed in 125nm static CMOS technology.

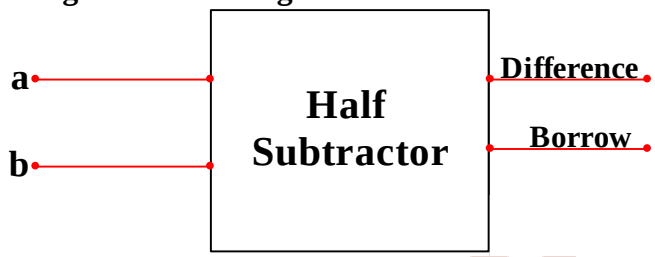
II. EXISTING SYSTEM:

A full Subtractor is a logic circuit build with two half subtractor. A half subtractor is a logic design in the combinational logic area in which it performs basic binary subtraction. A half subtractor is a two bit logical circuit .A half subtractor is made up of multiple gates which performs very basic operations according to the connections made in the CMOS (Complementary Metal Oxide Semiconductor).Full subtractor is also a two bit logical circuit. It consist of three inputs and two output where ‘a’, ’b’ and ‘c’ are considered to be inputs of the full subtractor whereas ‘difference’ and ‘borrow’ are the outputs of the the logical circuit.

Gates used in the full subtractor are ‘xor’ gate, ‘and’ gate, ‘not’ gate. Generally gate are the building blocks of the the combinational circuits .Gates are built using several numbers of transistor. We know that Moore’s law which states every six months number of the transistors used in a particular integrated circuit will be increased due to the technology enhancement. The XOR gate is a combinational logic gate that gives a ‘1’ output when the number of ‘1’ inputs is odd. An XOR gate implements an exclusive or, that is, a ‘1’ output results if one, and only one, of the inputs to the gate is ‘1’. If both inputs are ‘0’ or both are ‘1’, a ‘0’

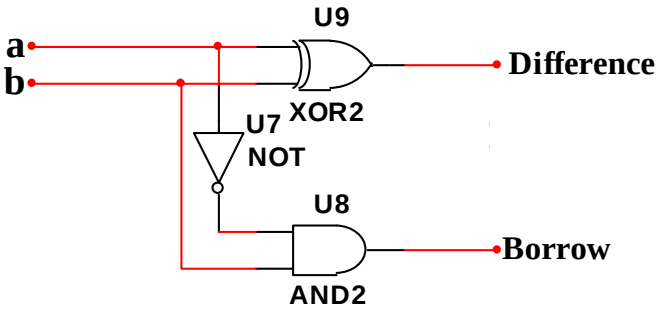
output results. In 'and' gate ,only multiplication operation can be done if the both input are same the output will be the same as the input and if the inputs are different then the output will '0'. In 'not' gate, contains only one input and the output is the output of the input if the input is '1' then the output will be '0' vice versa.

Fig-1.1: Block diagram of Half Subtractor:



In fig 1.1 we can analyze that a half subtractor consist of two inputs 'a' and 'b' and output 'difference' and 'borrow

Fig-1.2: Logic diagram of Half Subtractor:



In fig 1.2 Gates like 'xor', 'not', and 'and' Gates which are used to process the inputs and give the output. Each gate has a difference type of process algorithm based the connection given to the CMOS. The Boolean expression of the half subtractor is as follows

Difference = ab' + ba'

Borrow = a. b

Fig-1.3: Truth Table of Half Subtractor:

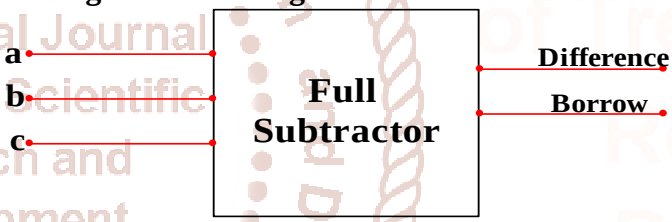
a	b	Difference	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

In fig 1.3 is a truth table of the half subtractor which portrays the output of that logical circuit. A half subtractor is a basic arithmetic processor which perform only subtraction its only function is to deduce a single bit binary from the input

III. FULL SUBTRACTOR:

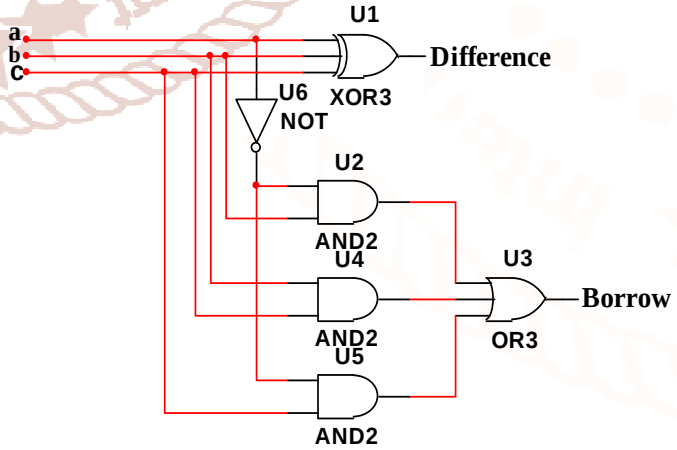
Half subtractor logical design has a major flaw in which we do not have the space to provide input bit for the subtraction in half subtractor. In case of full Subtractor logic, we can actually make a Borrow in input in the circuitry and could subtract it with other two inputs A and B. So, in the case of Full Subtractor Circuit we have three inputs, A which is minuend, B which is subtrahend and Borrow In. On the other hand we get two f output, Difference and Borrow. A full subtractor is basic combinatinal logic circuit which performs a single arithmetic function i.e. subtraction. It consist of three input naming 'a', 'b', 'c' which takes the input and process the algorithm using multiple gates such as 'xor', 'and' and 'not'. Comparison between currently existing full subtractor and newly area efficient full subtractor.

Fig2.1: Block diagram of Full Subtractor:



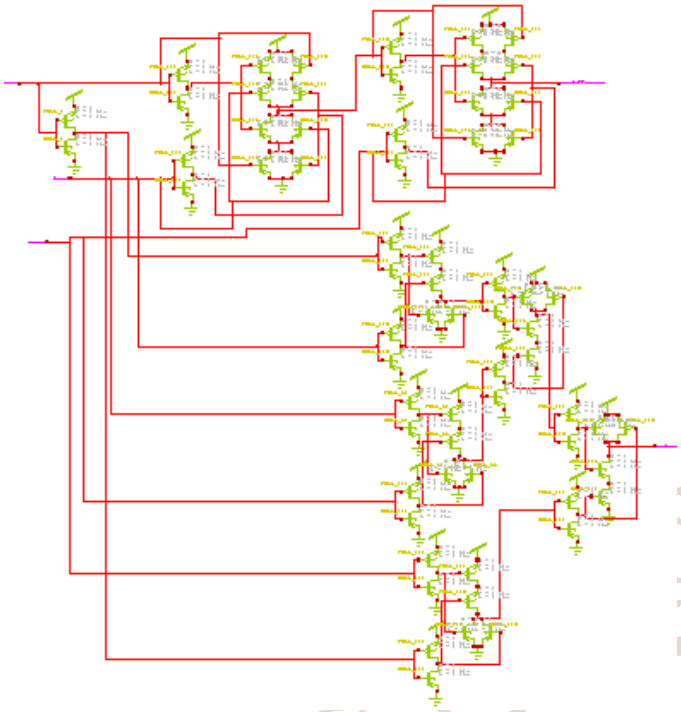
In fig 2.1 we can analyze that a full subtractor consist of two inputs 'a', 'b', and 'c whereas output 'difference' and 'borrow

Fig2.2: Logic Diagram of Full Subtractor:



When the inputs are given through the respective labels gates present the circuits will process the data and perform the arithmetic operation subtraction and produce the output difference and borrow

Fig2.3: CMOS Design of Full Subtractor:



The above full subtractor is designed using static cmos algorithm under 125nm which is quite efficient and the results are same as the currently existing one

Fig2.4: Truth Table of Full Subtractor:

a	b	c	Difference	Borrow
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

The above truth table is solved using the universal Boolean expression

Difference=((a&(~b)&(~c))| ((~a)&b&(~c))| ((~a)&(~b)&c)| (a&b&c))

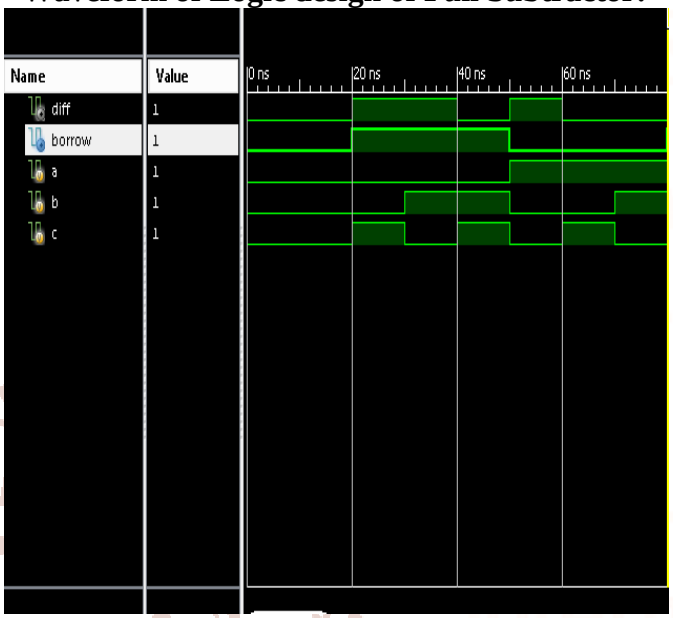
Borrow = ((~(a) & b) | (b & c) | (c & (~a)))

The above table used to serve the universal boolean expression of a logic gate function. A logic gate truth table shows each possible input combination to the gate or circuit with the final output depending upon the combination of these inputs.

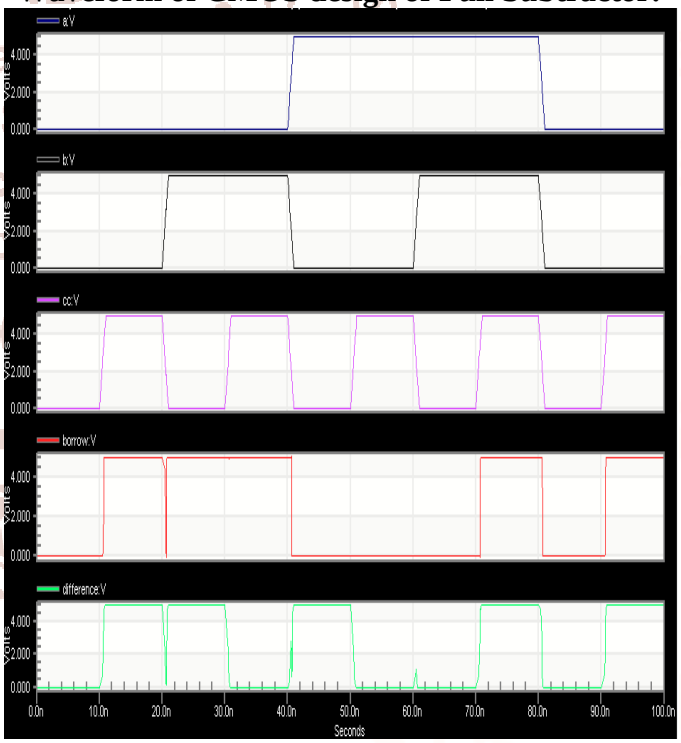
IV. RESULTS:

B.1 OUTPUT:

Waveform of Logic design of Full Subtractor:



Waveform of CMOS design of Full Subtractor:



CONCLUSION:

It has been observed from the simulation results that performance of adder architectures varies with various CMOS design. The output of these two designs of Full Subtractors are same. The current fabrication size of Carry Look Ahead adder is 125nm.If the fabrication size reduced to less than 100nm, the adder performance varies and can be absorbed using static (CMOS) technology. From this research the (CMOS)

can be achieved by operating point within 0.9v.This research is very useful and more advantageous in future microprocessor industries.

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