Efficient Design of 2:1 MUX (Multiplexer) using Nanotechnology Based on QCA

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ABSTRACT

Quantum Dot Cellular Automata is a new technology which overcomes of the of CMOS limitations. It is an novel advanced nano-technology that revolves around the single-electron position control. It is one of the most efficient and emerging nano-technology which mainly deals with the effect of electrons inside the quantum dots in QCA cell, and it is the best alternative technology in the nano-electronics level architectural field. In this paper, we designed a 2:1 Multiplexer, which is more efficient in the term of area and cells to the other designs.

Keyword: *Wire, Inverter, Majority Voter, CMOS, VLSI, Quantum dot cellular automata, Multiplexer, Quantum cell.*

I.   INTRODUCTION

QCA is a promising technology that provides a very efficient computational platform than CMOS is a nano-technology approach i.e. Quantum cellular automata (QCA) [1, 2]. It represents the digital information by polarization of electrons. It is attractive for its size, faster speed, feature, highly scalable, higher switching frequency and low power consumption compared to CMOS technology [4, 5, 6]. The four quantum dots form a QCA cell with one electron each in two of the four dots occupying "diametrically opposite" locations. Electrons occupy opposite (diagonal) corner quantum-dots because Coulomb repulsion is less compared to the scenario when they are in adjacent quantum dots [7, 8].
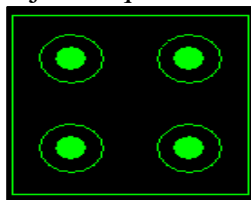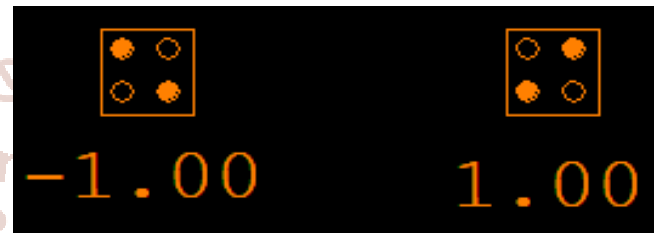

Fig. 1: Empty cell

(a): P = -1(Binary 0),   (b) P = 1(Binary 1)
Fig.2: Quantum-dots 90° cells polarizations

The new computing paradigm, QCA has been extensively studied in recent years. The basic element in Quantum dot cellular automata is a "cell" that consists of four metal islands dots known as QD [9, 10]. It's positioned at the corners of squared cell and two free charges [10].
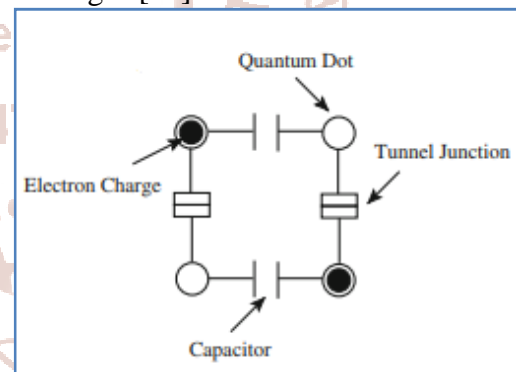

Fig. 3: Basic QCA Cell [10]

II.   MULTIPLEXER

A Multiplexers (MUX) is a combinational logic component that has several inputs and only one output. MUX directs one of the inputs to its output line by using a control bit word (selection line) to its select lines. A multiplexer can take any number of inputs line but then the selection line will be according to the number of inputs. The relation between the selection lines and the input lines is given in the equation 1.

$$2^M = N \qquad (1)$$

Where M is the selection lines and N is the number of input lines.

III. QCA DESIGN

Research on binary majority decision elements motivated by the development of devices such as parametrons and Esaki diodes has been reported as early as 1960. The majority function or majority voter consist of only three input QCA cells implements the logic function is Eq. 2. Where A, B, and C are inputs and F is the single output as shown in fig. 8. The basic element of QCA is wire is shown in figure 4, inverter in figure 6.

$$F = AB + BC + AC \qquad (2)$$
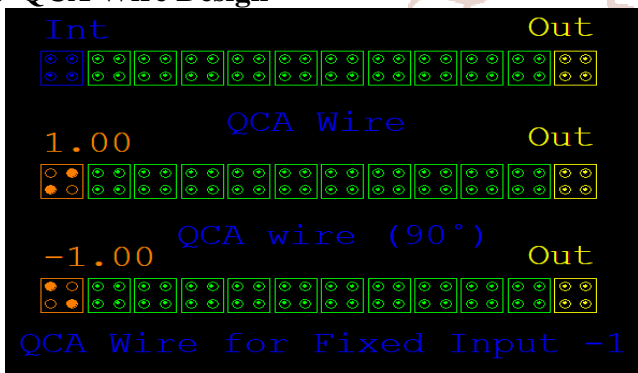
A. QCA Wire Design

Fig. 4: QCA Design for Wire using 12 Quantum Cells as consider 90^0 (Normal cell) cell
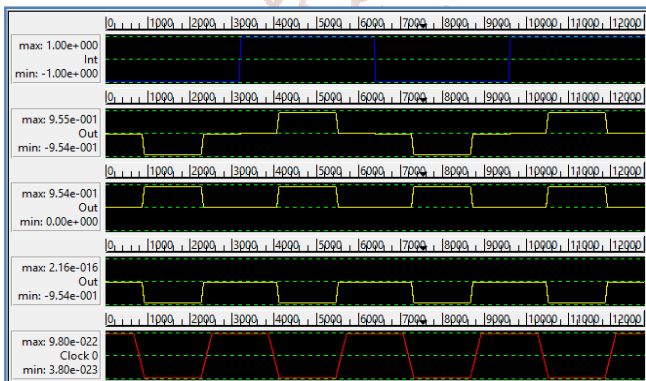

Fig. 5: Simulation result for QCA wire as consider Normal cell for 90^0
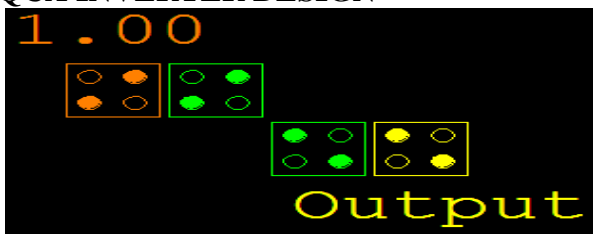
B. QCA INVERTER DESIGN

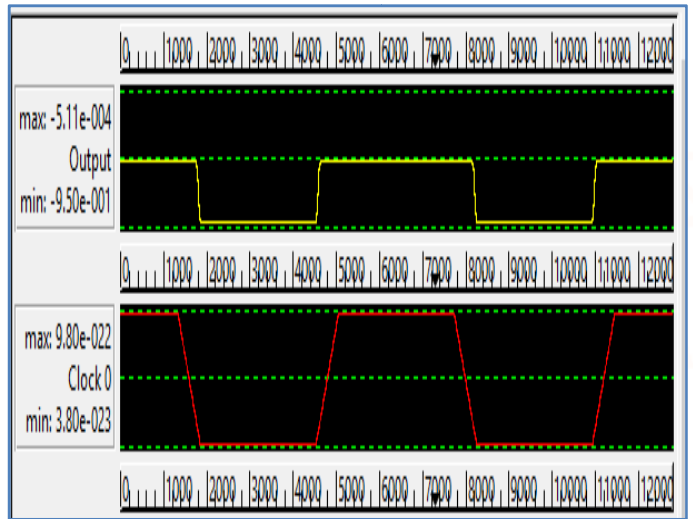**Fig. 6: Layout of an "alternate inverter" configuration**

Fig. 7: Simulation result for an "alternate inverter" configuration
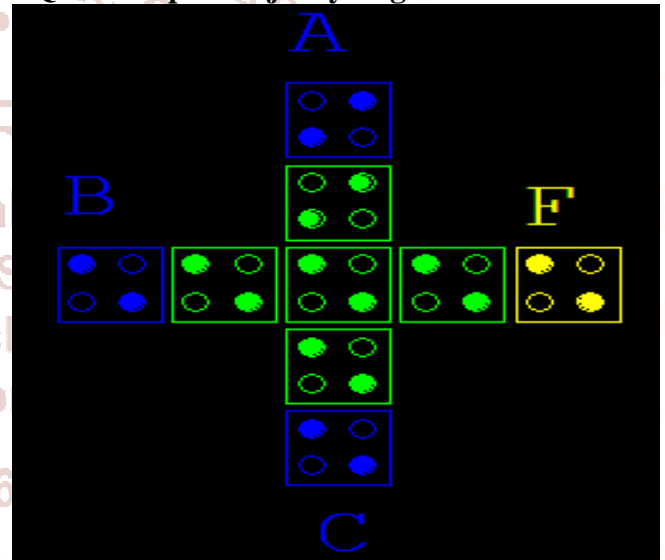
C. QCA 3-Input Majority Logic

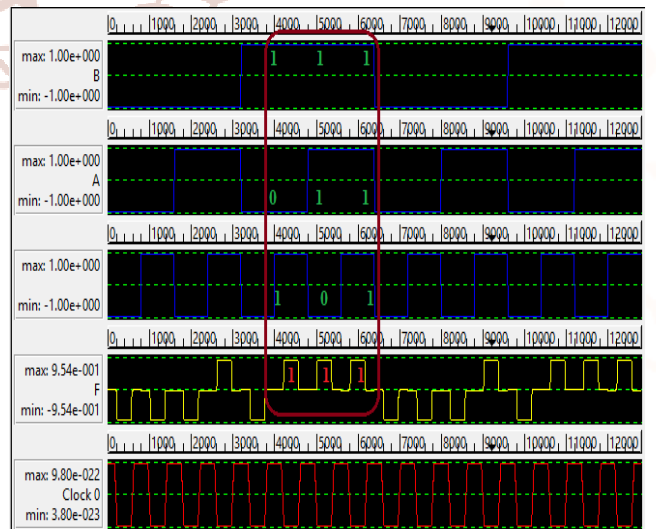**Fig. 8: Layout of majority voter (MV) consist of three input QCA cells**

Fig. 9: Simulation result for majority voter (MV) consist of three input QCA cells

IV. Bi-STABLE SIMULATION PARAMETERS

To verify our proposed layout designs of different logic gates on used recent specific resolution tool QCA Designer version 2.0.3 with the bistable simulation engine setup.

Table 1: Bistable Simulation Parameters

Parameter	Value	
Cell width	18nm	Layer Properties
Cell height	18nm	
QCA-Quantum-dot diameter	5nm	
Default Clock	Clock 0	
Time-step	1.0e-16s	Bistable Approximation (Options)
Relaxation time	1.0e-15s	
Clock-low	3.8e-023J	
Clock-high	9.8e-022J	
Radius of effect	65nm	
Relative permittivity	12.90	
Layer separation	1 1.50nm	

V. PROPOSED DESIGN

The truth table of the 2-to-1 multiplexer is shown in table 2. depending on the selector (S) switching the inputs are produced at outputs , i.e., D_0 , D_1 and are switched to the output for S=0 and S=1 respectively . Thus, the Boolean expression for the output becomes D_0 when S=0 and output is D_1 when S=1. From the truth table the Boolean expression of the output Y is given as:

$$Y = D_0\bar{S} + D_1S \qquad (3)$$

Table 2: Truth table for 2:1 MUX

Select	Inputs		Output
S	A	B	Y
0	0	0	0
0	0	1	1
1	1	0	1
1	1	1	1

This is because of its ability to select one signal out of many inputs. We are proposed 2:1 MUX design in figure 10 based on quantum cells shown in figure 10

first proposed design, quantum cells 24, used design area in 0.04 µm^2.
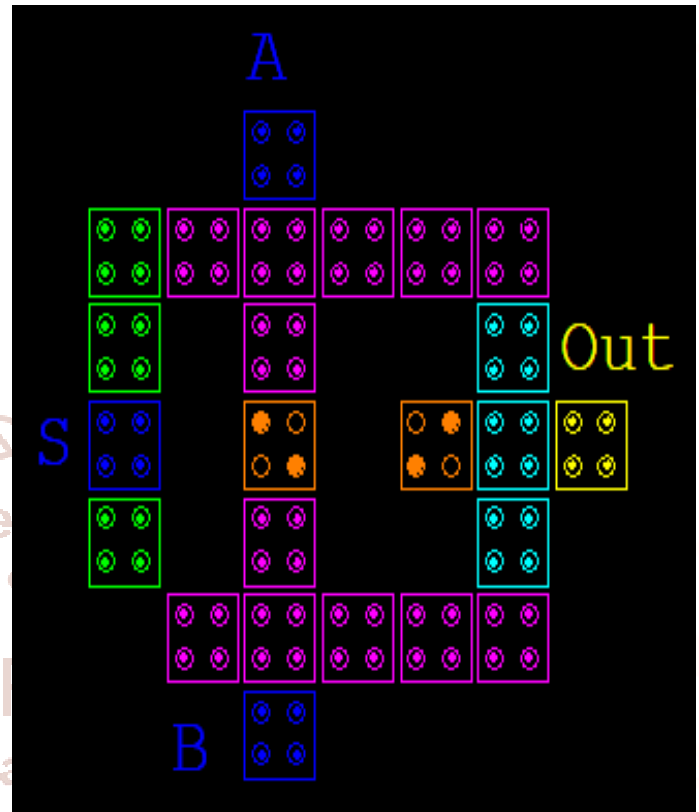
Fig. 10: First proposed 2:1 multiplexer design using 24 Quantum cells
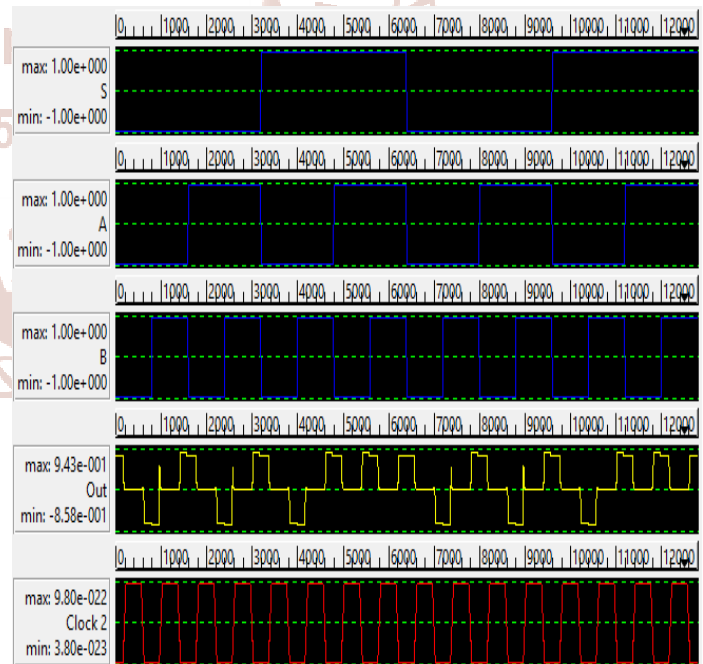

Fig. 11: Simulation Output for 2:1 multiplexer design using 24 Quantum cells

Result Analysis: Selection extents: (156.19, 150.31) [228.04x162.88] = 37142.55 nm^2 = 0.04 µm^2 Objects selected: 24.

Table 3: The comparative table for the 2:1 QCA multiplexer architectures

Authors Name	Number of Cells	Area	Clock Delay	Wire Crossing
V.A. Mardiris et al. [4]	56	0.07	4	Coplanar
A. Roohi et al. [5]	27	0.03	3	Coplanar
R. S. Nadooshan et al. [7]	26	0.02	3	Coplanar
Proposed Design-1 [Fig. 10]	24	0.03	2	Coplanar

VI. CONCLUSION

The MUX are important part of digital logical circuits and control systems. In this paper, proposed designs for QCA 2:1 MUX were reviewed. The functionality of the proposed circuits is necessary to validate the designs using the QCA Designer bistable engine [10]. The proposed design, in term of cells, has better operation compared to the other existing some designs.

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