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Performance Improvement of QCA Design XOR Logic Gate using Bistable Simulation Engine Vector

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ABSTRACT
Among the emerging technologies recently proposed as alternatives to the CMOS technology, the quantum-dot cellular automata is one of the promising solutions to design very high speed and ultralow power digital circuits. In this paper we used QCA Designer simulator tool for simulation of the proposed XOR design. The QCA Designer tools used to simulate the circuits and calculate the area as well as number of cells.

Keyword: *QCA, XOR, Majority Gate, QCA Cells, Bistable Simulation Engine.*

I. INTRODUCTION
QCA is a computational nanotechnology that can be used to construct nano-scale circuits. Nowadays, this technology is a popular alternative for CMOS technology due to features such as speed, low occupied area and low power consumption [1]. The many technologies have been investigated such as Carbon Nano Tube field effect transistors (CNTFETs), Single electron transistors (SETs), Quantum-dot cellular automata (QCA) and others. QCA is a promising technology supporting a transistor-less paradigm. This QCA technology has quantum cells. The quantum cells has 2 electrons present at a time, has 4 quantum wells and 2 electrons are occupies in adjacent position to each other. The rest of paper is organised in section A.1 is QCA building blocks, II-Section QCA clock diagram dissection, Section-III Simulation design and results and last section IV is conclusion and references at the last of paper.

A. QCA building blocks
The building blocks are determined by the fundamental logic gate structure. Each QCA cell contains two electrons and four quantum dots and due to Coulomb interaction between these identical charges, they occupy dots diagonally. As a result, the two stable polarization states for a QCA cell are achieved, as shown in Figure 1. The instantaneous polarization of a cell is denoted as either -1 or +1 [2], which are encoded to represent a binary "1" value and "0" value, respectively. In order to create any digital logic, basic elements including wire, NOT gate, AND gate, OR gate and majority gate are required to implement that logic [1, 3]. Since no electrons tunnel between cells, QCA provides a mechanism for transferring information without current flow [6].

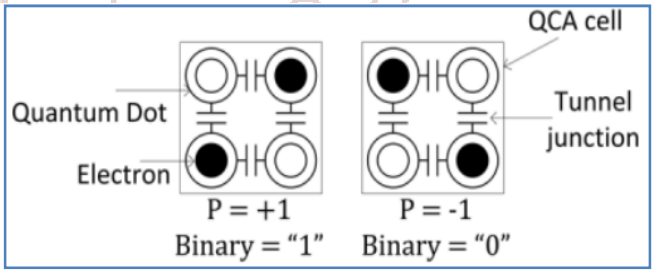

Fig.1: Basic QCA cell with two binary state [7]

The Majority voter (M), five QCA cells that realize the function of in equation 1, and its QCA design is shown in figure 2.

$$M\,(a,b,c) \;=\; ab + bc + ac \quad (1)$$

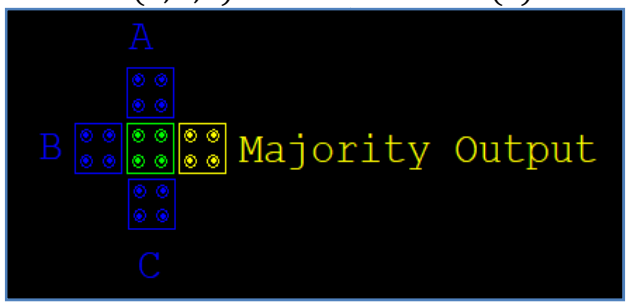

Fig. 2: MV QCA Design

For example, a two-input AND gate is realized by fixing one of the majority gate inputs to "0," that is in equation 2,

$$AND\ (a,b) = M\ (a,b,0) = a.b \quad (2)$$

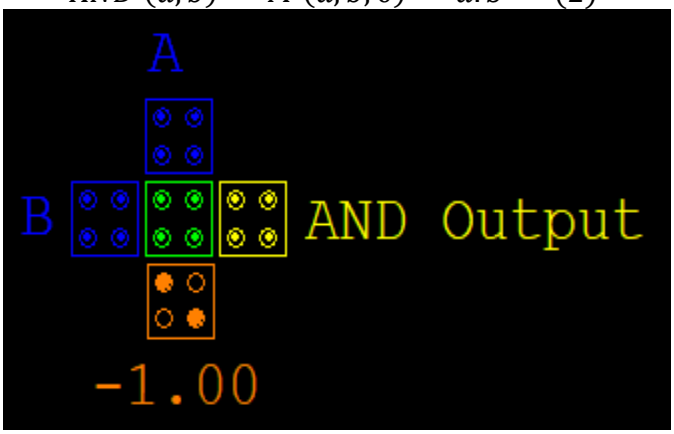

Fig. 3: AND Logic Gate using QCA Cells

Similarly, an OR gate is realized by fixing one input to "1," that is in equation 3,

$$OR\ (a,b) = M(a,b,1) = a + b \quad (3)$$

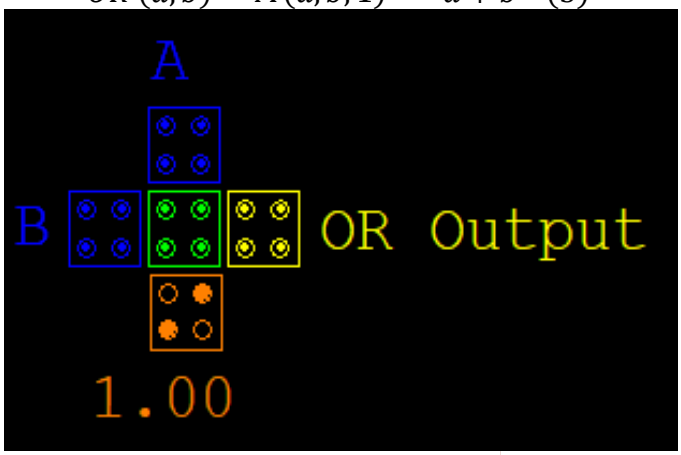

Fig. 4: QCA OR Logic Gate

II. QCA CLOCK

In QCA technology, storage cells do not require an external power source to maintain their current stable polarization. Actually, the clock controls the flow of charge in the circuit. The QCA clock consists of four clock phases, i.e. Switch, Hold, Release, and Relax, which span a 90 degree out-of phase progression [4, 5]. It is shown in figure 5 for QCA clock diagram. This diagram x-axis represents the time and Y-axis represents the inter-dot-barrier.

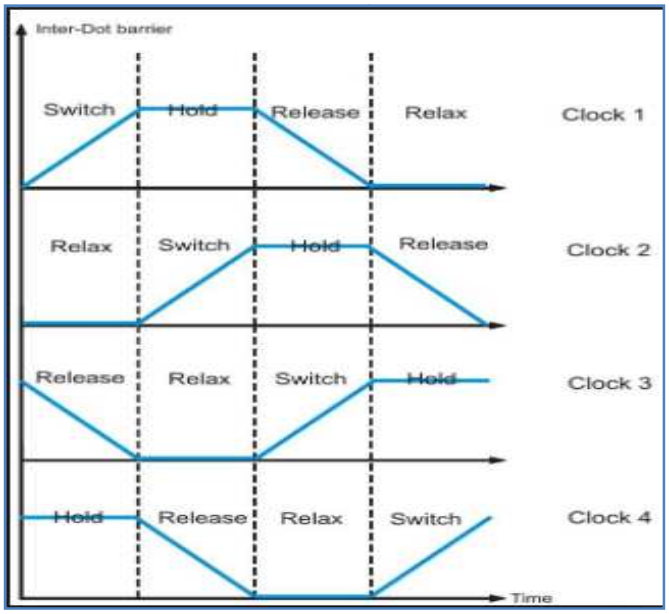

Fig. 5: QCA Clock [7]

III. SIMULATION RESULTS

We are proposed two different QCA "XOR logic design" in figure 4.5 XOR-1 with using Quantum cells 27 used design area in 0.04 μm^2 with utilized single layer design and clock cycle delay count one. This design is efficient in team of design cell area as well as used cell count.

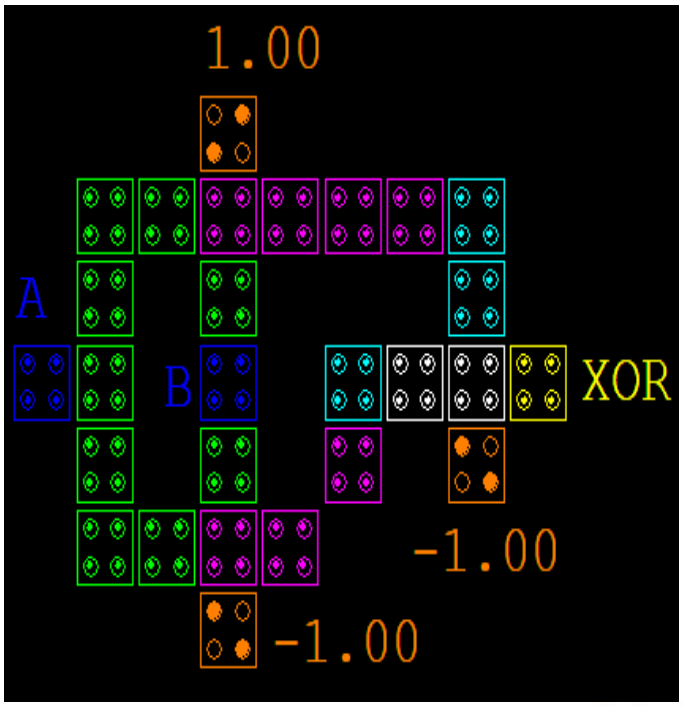

Fig. 6: Proposed QCA-XOR Logic Gate Design

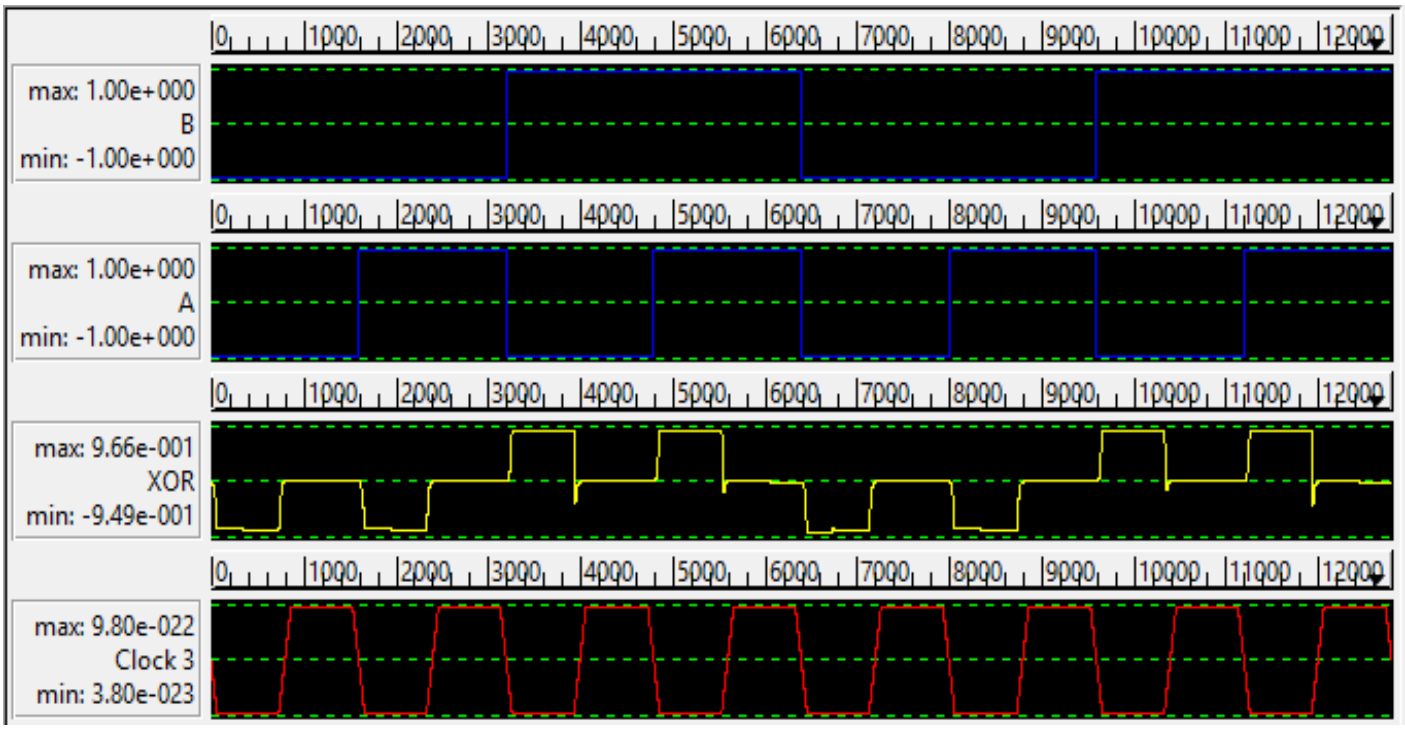

Fig. 7: Simulation of XOR Logic Gate

Table 1: Comparison of Proposed Design and Previous design of QCA XOR

Design	Cell	Area	Delay
Proposed Design XOR	27	0.04	1
Mrinal Goswami (2014) et al. [9]	40	0.04	3
Young-Won You (2016) et al. [10]	44	0.05	4

IV. CONCLUSIN

CMOS technology is approaching its scaling limit very fast. Quantum-dot Cellular Automata (QCA) is an emerging nanotechnology, with extremely small feature size and ultra low power consumption compared to transistor-based technology. The proposed design results analysis is shown in table 1 in this table we compared the both design XOR logic gate on the bases of quantum cells, design area and delay. The proposed design used the bistable simulation engine.

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