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A Design and Implementation of Reversible Logic Based Combinational Circuit with Low Quantum Cost

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ABSTRACT

In the field of cryptography, optical information processing low power CMOS design and nanotechnology Reversible logic has found its applications and has become one of the promising research directions this paper presents a novel and quantum cost efficient combinational circuits for nanotechnology. This gate can work singly as a reversible full adder unit and requires only one clock cycle. The proposed gate is a universal gate in the sense that it can be used to synthesize any arbitrary Boolean functions. It has been demonstrated that the hardware complexity offered by the proposed gate is less than the existing counterparts. The proposed reversible circuits are then compared with different reversible circuits

Keywords: *Component, floating point adder, reversible logic, reversible logic*

1. INTRODUCTION

Power dissipation is one of the most important factors in VLSI circuit design. Irreversible logic circuits dissipates kT*log 2 Joule (k is the Boltzmann constant and T is the absolute temperature) heat for every

bit of information that is lost irrespective of their implementation technologies [1]. Information is lost when the input vectors cannot be recovered from circuit's output vectors. Reversible logic naturally takes care of heating since in reversible circuits the input vectors can be uniquely recovered from its corresponding output vectors. Bennett [2] showed that zero energy dissipation is possible only if the gating network consists of reversible gates. Thus reversibility will become future trends towards low power dissipating circuit design.

Reversible logic design differs significantly from traditional combinational logic design approaches. In reversible logic circuit the number of input lines must be equal the number of output lines, each output will be used only once and the resulting circuit must be acyclic [3]. The output lines that are not used further are termed as garbage outputs. One of the most challenging tasks is to reduce these

garbages [3]. Any reversible logic gate realizes only the functions that are reversible. But many of the Boolean functions are not reversible. Before realizing these functions, we need to transform those irreversible functions into reversible one. Any transformation algorithm that converts an irreversible function to a reversible one introduces input lines that are set to zero in the circuit's input side [4-5]. These inputs are termed as constant inputs. Therefore, any efficient 0.....reversible logic design should minimize the garbages as well as constant inputs.

This paper presents a novel 4*4 reversible gate namely Peres Full Adder Gate (PFAG) , that is, it has 4-input lines and 4-output lines. This gate can be used to realize any arbitrary Boolean function and therefore

universal. The hardware complexity of this gate is less compared to the existing ones and requires only one clock cycle. The quantum realization cost of this gate is only 8 and ready for use in

Table 1.1

Truth table of Irreversible X-OR Gate

A	B	P
0	0	0
0	1	1
1	0	1
1	1	0

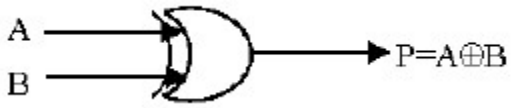

Figure 1.1: Irreversible EX-OR Gate

Table 1.2

Truth table of Reversible X-OR Gate

A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Here P represents the Garbage output

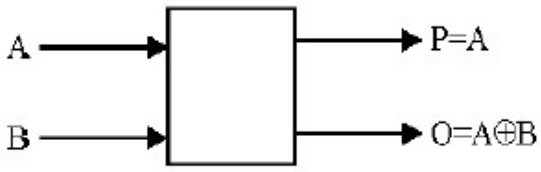

Figure 1.2: Reversible EX-OR Gate

II. REVERSIBLE LOGIC GATES

There exist many reversible gates in the literature. Among them 2*2 Feynman gate [6] (shown in figure2), 3*3 Fredkin gate [7] (shown in figure 2.2), 3*3 Toffoli gate [8] (shown in figure 2.3) and 3*3 Peres gate [9] (shown in figure 2.4) is the most referred. The detailed cost of a reversible gate depends on any particular realization of quantum logic. Generally, the cost is calculated as a total sum of 2*2 quantum primitives used. The cost of Toffoli gate is exactly the same as the cost of Fredkin gate and is 5. The only cheapest quantum realization of a complete (universal) 3*3 reversible gate is Peres gate and its cost is 4.

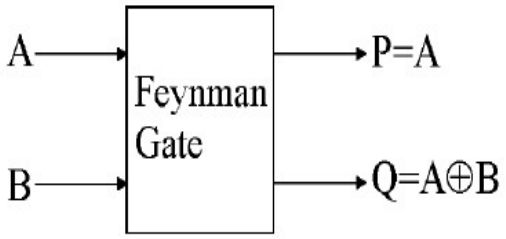

Figure 2.1: 2*2 Feynman Gate

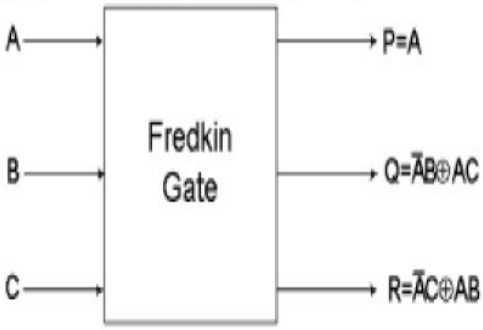

Figure 2.2: 3*3 Fredkin Gate

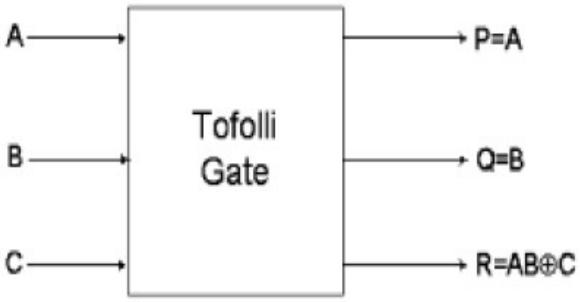

Figure 2.3: 3*3 Tofolli Gate

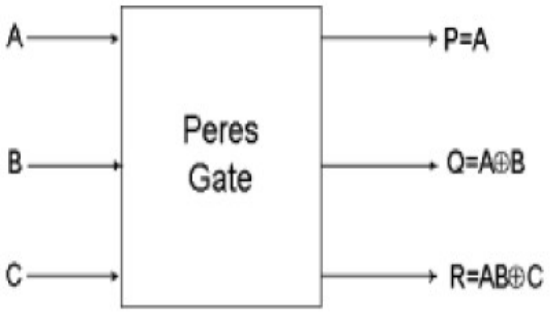

Figure 2.4: 3*3 Peres Gate

III Reversible Logic Implementation of Combinational Circuit

A. Design of 1 bit Full Adder

Full adder is the fundamental building block in many computational units. The anticipated paradigm shift logic compatible with optical and quantum requires compatible reversible adder implementations. The full adder circuit's output is given by the following equations:

Sum = A □□B □□Cin□

Cout = (A □□B) Cin □□AB

The reversible logic implementation of full-adder circuit and other adder circuits and their minimization issues has been discussed in . It has been shown in [11] and [13] that any reversible logic realization of full adder circuit includes at least two garbage outputs and one constant input. The author in [10-13] has given a quantum cost efficient reversible full adder circuit that is realized using two 3*3 Peres gates only (shown in figure 3.1). This implementation of reversible full adder circuit is also efficient in terms of gate count, garbage outputs and constant input than the existing counter parts.

For this implementation, I will be using the Peres gate as it is the gate with the lower quantum cost as can be seen in the figures 3.1. The Peres' implemented Full Adder with its corresponding quantum cost can be seen below:

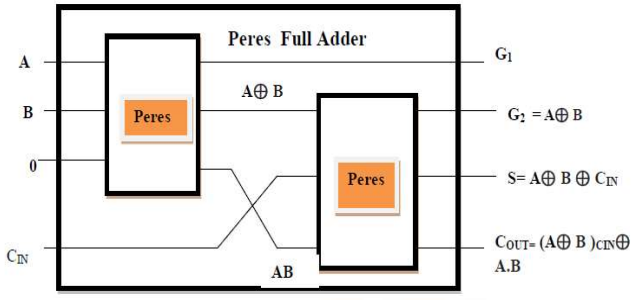

Figure 3.1 Peres Full Adder

This PFA (Peres Full Adder) can be taken as a block in order to facilitate the notation of its expansion. The inputs order was also changed to better fit in an expansion diagram.

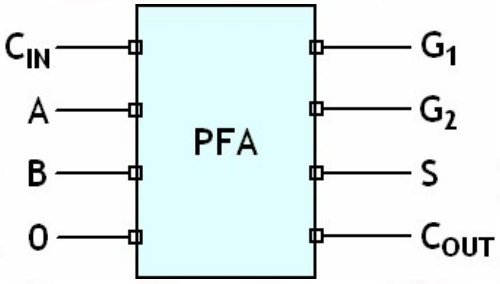

Figure 3.2 PFA as a block

Once we take the FPA as a block, we can derive the algorithm to implement an n-bits adder. This algorithm was implemented in this design and can be seen in figure 3.3

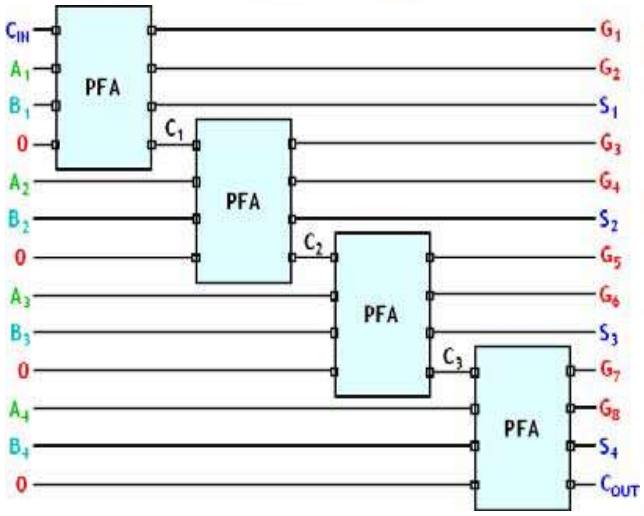

Figure 3.3: 4-bits adder implementation

B. Design of 2x4 reversible decoder with low quantum cost and minimum garbage output.

Figure below shows the circuit of 2x 4 decoder using one feyman gate and two modified fredkin gate. The quantum cost of modified fredkin gate is 4[12]. For given inputs corresponding outputs are resulted as x,y,w,z.

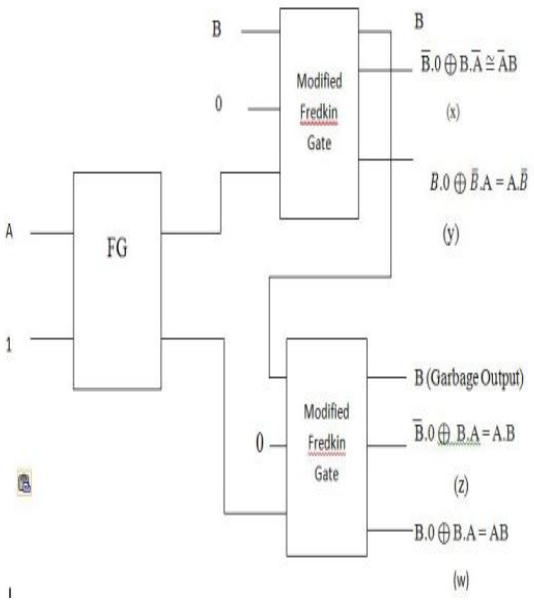

Figure .3.4: 2x4 reversible decoder

C. Design of 3x8 reversible decoder

Table 3.1 Truth table of 3x8 reversible decoder

A	B	C	x_0	x_1	x_2	x_3	x_4	x_5	x_6	x_7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

Table above shows the truth table for 3x8 reversible decoder and figure below shows the circuit of 3x 8 decoder using one feyman gate and six modified fredkin gate. The quantum cost of modified fredkin gate is 4[12]. For given inputs corresponding outputs are resulted as x0 ,x1,x2,x3,x4,x5,x6,x7.

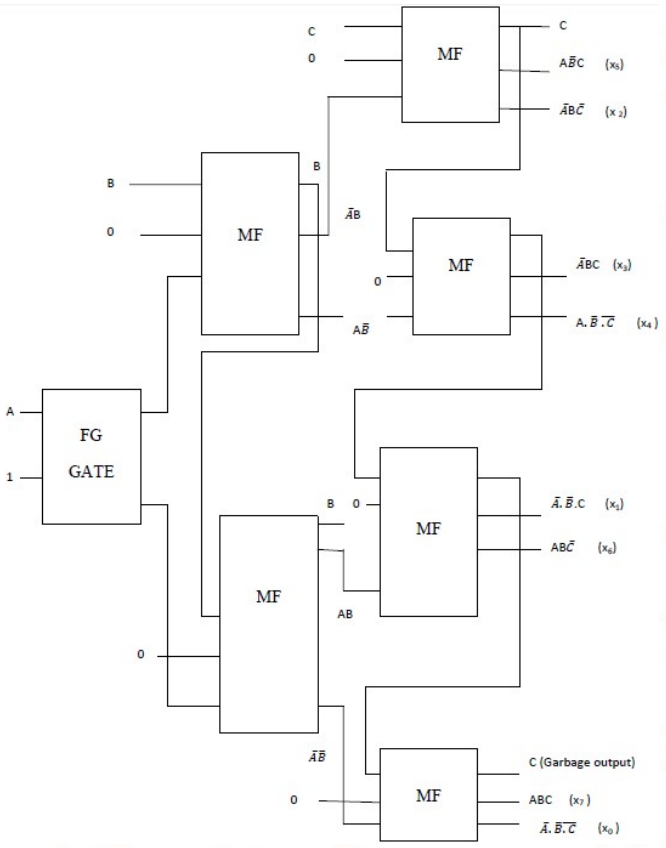

Figure 3.5: Reversible 3X8 decoder

IV. Result and Simulation

The venture was reenacted with the assistance of the Xilinx ISE 9.2 instrument.

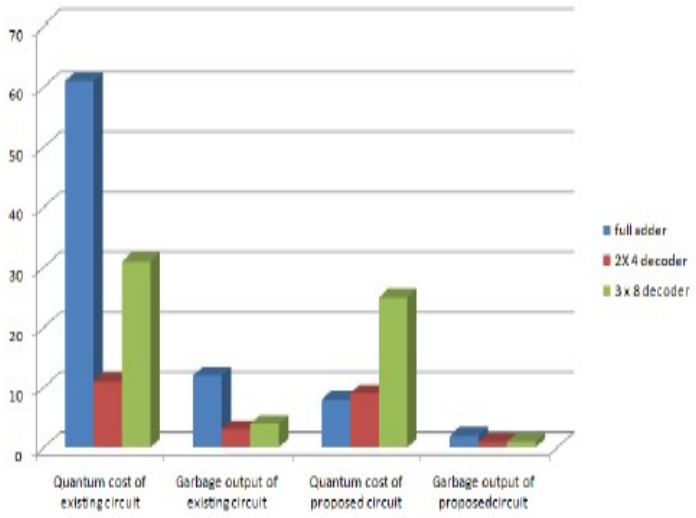

Figure 4.1 Graph showing comparison in existing and proposed quantum cost and garbage output

The combinational circuit full adder is designed using peres gate and 2x4 decoder , 3x8 decoder is designed using modified feyman gate and modified fredkin gate are analyzed in terms of quantum cost and garbage output.

Table 4.1

Comparison between quantum cost and garbage output

CIRCUIT	QUANTUM COST OF EXSISTING CIRCUIT	GARBAGE OUTPUT OF EXSISTING CIRCUIT	QUANTUM COST OF PROPOSED CIRCUIT	GARBAGE OUTPUT OF EXSISTING CIRCUIT
FULL ADDER	61	12	8	2
2 X 4 DECODER	11	3	9	1
3 X 8 DECODER	31	4	25	2

The figure below shows the RTL view of 1 bit full adder with low quantum cost and minimum garbage output

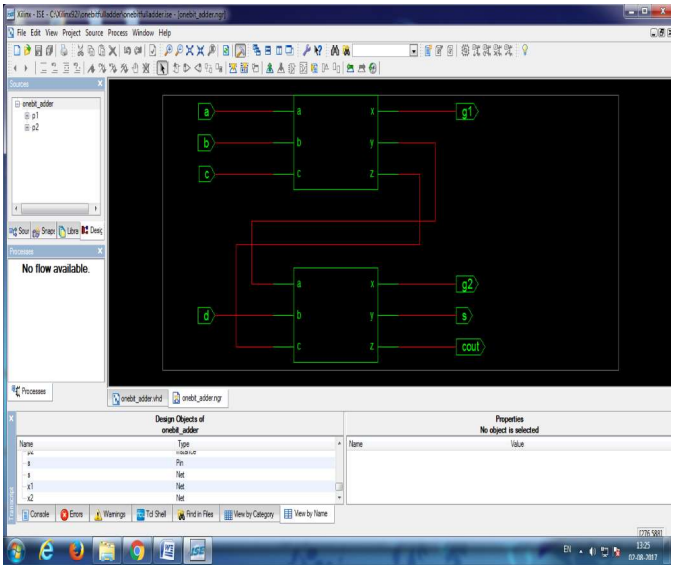

Figure 4.2 RTL Schematic of 1 bit full adder

Figure below shows the simulation result of 1 bit full adder with low quantum cost and minimum garbage output [1].From simulation result of 1 bit full adder we can check the desired output of full adder by assigning different combination of inputs and it can be checked with the truth table of full adder if our outputs are same as the output of the truth table for different combination our simulation of full adder is correct.

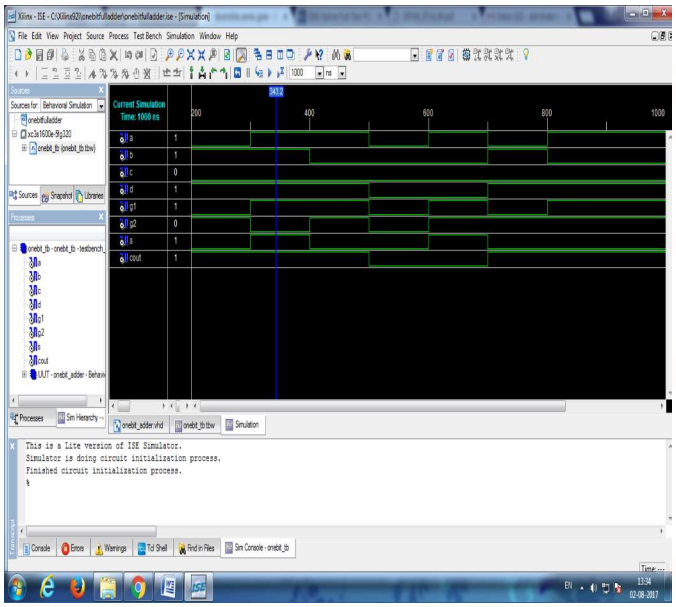

Figure 4.3 Simulation result of 1 bit full adder

The figure below shows the RTL architecture of 3x8 decoder with minimum quantum cost and garbage output

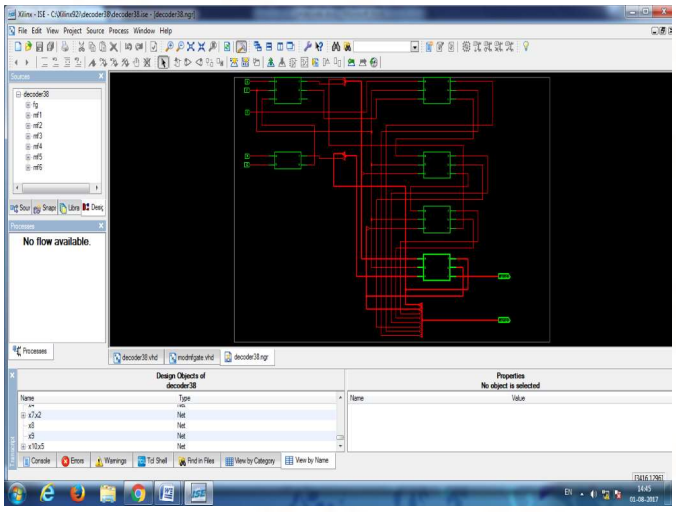

Figure 4.4 RTL Schematic of 3x8 reversible decoder

Figure below shows the simulation result of 3x8 decoder with low quantum cost and minimum garbage output [1].From simulation result of 3x8 decoder we can check the desired output of decoder by assigning different combination of inputs and it can be checked with the truth table of decoder if our outputs are same

as the output of the truth table for different combination our designed circuit is correct.

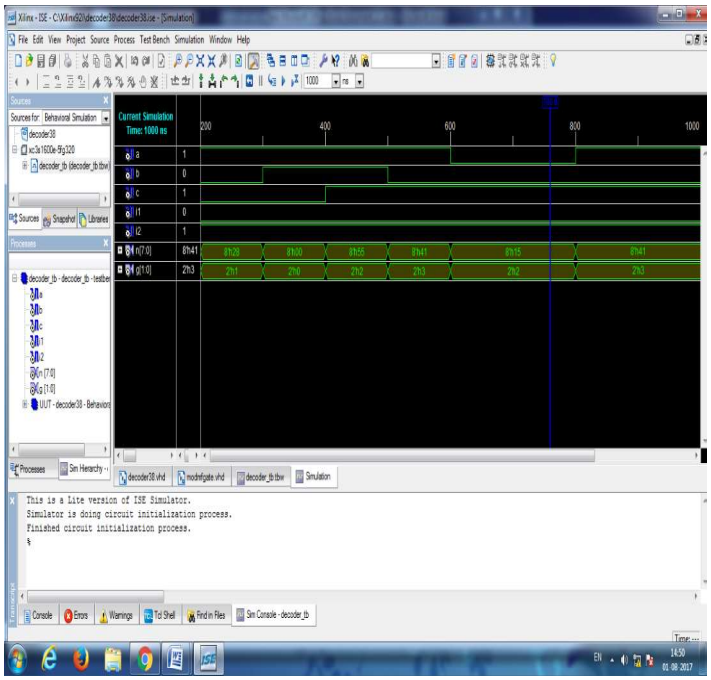

Figure 4.5: Simulation of 3 x 8 reversible decoder

2X4 Reversible decoder

The figure below shows the RTL architecture of 2X4 decoder with minimum quantum cost and garbage output [1]

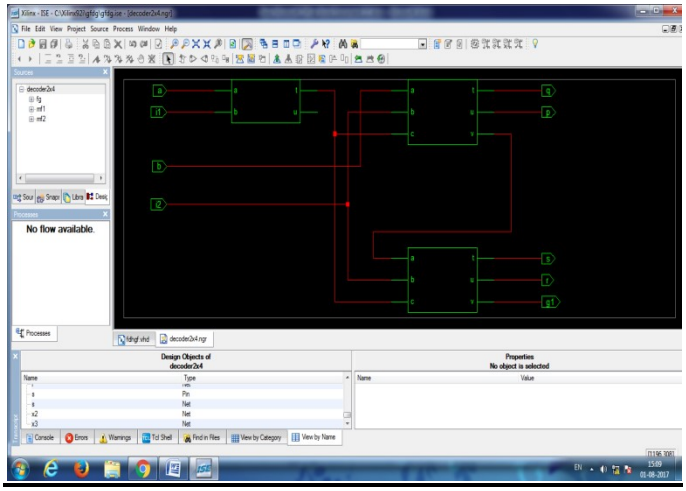

Figure 4.6 RTL View of 2x4 decoder

Simulation result of 2:4 decoder

Figure below shows the simulation result of 2x4 decoder with low quantum cost and minimum garbage output [1].From simulation result of 2x4 decoder we can check the desired output of decoder by assigning different combination of inputs and it can be checked with the truth table of decoder if our outputs are same as the output of the truth table for different combination our designed circuit is correct.

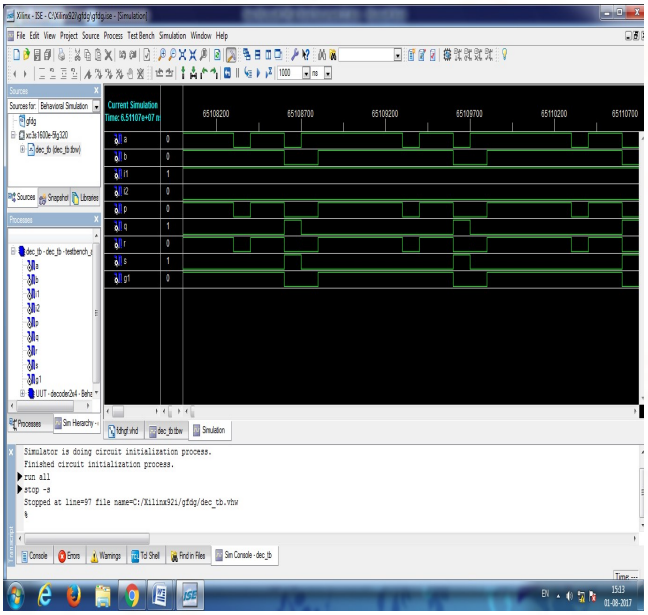

Figure 4.7: Simulation result of 2x4 decoder

CONCLUSION

In this dissertation combinational circuit like full adder, 2x4decoder, 3x8decoder are designed using reversible gate. These circuits are designed for minimum quantum cost and minimum garbage output. The method proposed can be generalized. The method of designing combinational circuit helps to implement many digital circuits with better performance for minimum quantum cost and garbage output. Future work related to building of proposed reversible logic by using technologies such as CMOS technology, in particular adiabatic CMOS, optical, thermodynamics, technology, nanotechnology and DNA technology is another important aspect.

REFERENCES

[1] Gopi chand Naguboina et al: "Design and synthesis of combinational circuit using reversible decoder in Xilinx. IEEE Xplore 2017 intenational conference.

[2] H M H Babu, M R Islam, S M A Chowdhury: Synthesis of full-adder circuit using reversible logic. 17th International Conference on VLSI Design. Proceedings. IEEE Xplore**:** 24 August 2004

[3]Junchaw Wing, Ken Choi: A Carry look ahead adder designed by reversible logic. SoC Design Conference (ISOCC), 2014 International **IEEE Xplore:** 20 April 2015

[4] Marcin Bryk , Krzysztof Gracki , Paweł Kerntopf , Marek Pawłowski , Andrzej Skorupski: Encryption using reconfigurable reversible logic gate and its simulation in FPGAs; Mixed Design of Integrated Circuits and Systems, 2016 MIXDES - 23rd International Conference **IEEE Xplore:** 04 August 2016

[5]R. Keyes and R. Landauer : "Irreversibility and Heat Generation in the Computational Process*", IBM Journal of Research and Development,* vol. 5, pp. 183-191, 1961

[6] W David Pan, Mahesh Nalasani; Reversible logic; IEEE Potentials (Volume: 24, Issue:Feb.-March 2005)

[7] H.Thapliyal and N. Ranganathan. Reversible logic based concurrent error detection methodology for emerging nanocircuits. In Nanotechnology (IEEE-NANO) 10th IEEE Conference on, pages 217 – 222, aug. 2010.

[8]Design of a Reversible Floating-Point Adder Architecture by Michael Nachtigal and all in 2011 11th IEEE International Conference on Nanotechnology Portland Marriott

.

[9]Design of a Reversible Floating-Point Adder Architecture by Michael Nachtigal and all in 2011 11th IEEE International Conference on Nanotechnology Portland Marriott.

[10] C H Bennet "Logical reversibility of computation" IBM Journal and dev, pp525-532 nov 1973

[11] Anindita Banerjee et al. "New design of reversible sequential devices" 12 august 2009

[12] Ankush et al "Design and performance analysis of low power reversible carry skip adder" IOSR Journal of VLSI and signal processing.

[13] Anupam Chattopadhyay, Anubha Bhakshi " Low quantum cost constructions for adder and symmetric Boolean function" 2016 International symposium on circuits and system, IEEE xplore 11 aug 2016.