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Simulation of 16 bit ALU using Verilog-hdl

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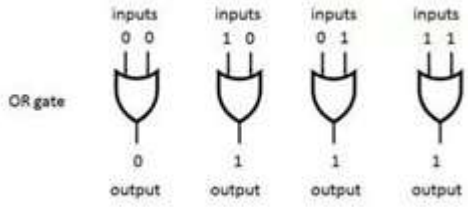
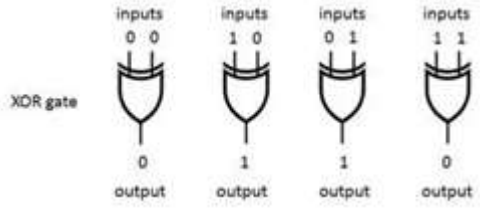
ABSTRACT

In many digital circuits ALU is a basic building block. It can be used in integer arithmetic computations and as Complex operation. This research paper is based on the simulation of 16 bit ALU using VHDL. The design was implemented using VHDL Xilinx Synthesis tool ISE and targeted for Spartan device. An ALU performs following operations – Addition, subtraction, multiplication, Not, logical shift right, logical shift left, rotate right, rotate left, OR, AND, XOR, NAND, NOR, XNOR and comparison between two signals.

INTRODUCTION

An arithmetic logic unit (ALU) is a combinational digital electronic circuit that performs arithmetic and bitwise operations. It represents the fundamental building block of the central processing unit (CPU) of a computer. Modern CPUs contain very powerful and complex ALUs. An ALU performs basic arithmetic and logic operations. Examples of arithmetic operations are addition, subtraction, multiplication, and division. Examples of logic operations are NOT, AND, and OR. All operations perform in a computer is in form of binary number i.e. 0 or 1. The logical operations are given below-





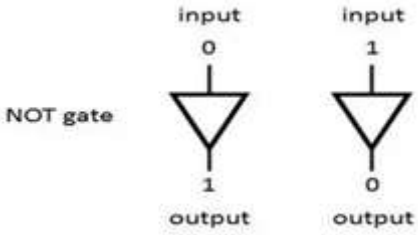


Table for different operation-

Option	operation
0000	Addition
0001	Subtraction
0010	Multiplication
0011	Not
0100	Logical shift left
0101	Logical shift right
0110	Rotate left
0111	Rotate right
1000	And
1001	Or
1010	Xor
1011	Nor
1100	Nand
1101	xnor
1110	Greater comparison
1111	Equal comparison

Table 2.1

RTL schematic of ALU

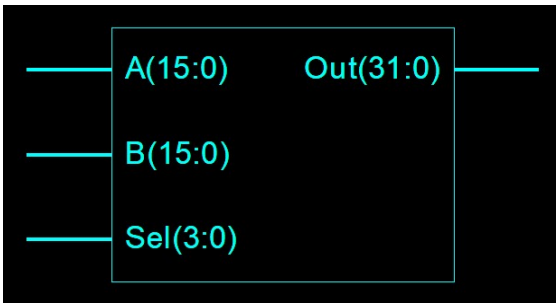


Figure: 2.1

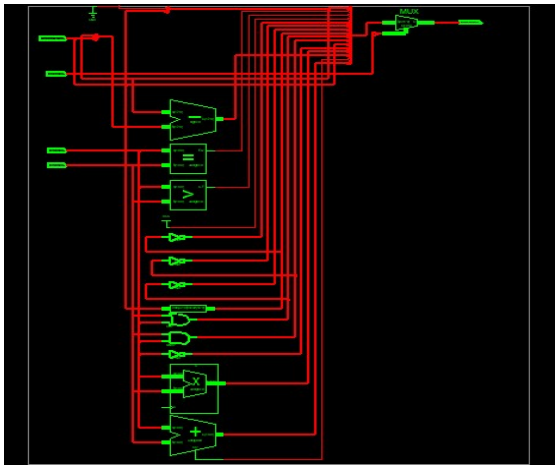


Figure: 2.2

Result

Verilog hdl implementation of ALU was done using Xilinx ise. Detailed report is given below in table no. 3.1.

Logic utilization	used	Available	utilization
Number of Slices	102	2448	4%
Number of 4 input LUTs	192	4896	3%
Number of bonded IOBs	68	108	62%
Number of MULT18X18SIOs	1	12	8%

Table: 3.1

The time delay and memory usage is given in table no. 3.2

Delay	12.339ns
Memory usage	235436 kilobyte

Table 3.2

CONCLUSION

The simulation of 16 bit ALU is presented. This design is implemented using Verilog hdl and Xilinx ise and targeted for Spartan 3e family. The time delay is 12.339ns and memory usage is 235436 kilobyte.

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